

**AD-A277 293**



**NAVAL POSTGRADUATE SCHOOL**  
**Monterey, California**

2



**DTIC**  
**ELECTE**  
**MAR 28 1994**  
**S F D**

**THESIS**

**RADIATION TOLERANT,  
HIGH SPEED, LOW POWER,  
GALLIUM ARSENIDE LOGIC**

by

Kurt Wolfe

December, 1993

Thesis Advisor:

Douglas J. Fouts

Approved for public release; distribution is unlimited.

**94-09396**



DTIC QUALITY ASSURED

**94 8 25 09 8**

REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188	
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington DC 20503				
1. AGENCY USE ONLY (Leave blank)		2. REPORT DATE 16 December 1993.		3. REPORT TYPE AND DATES COVERED Master's Thesis
4. TITLE AND SUBTITLE RADIATION TOLERANT, HIGH SPEED, LOW POWER, GALLIUM ARSENIDE LOGIC.			5. FUNDING NUMBERS	
6. AUTHOR(S) Kurt A. Wolfe				
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey CA 93943-5000			8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)			10. SPONSORING/MONITORING AGENCY REPORT NUMBER	
11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.				
12a. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution is unlimited.			12b. DISTRIBUTION CODE A	
13. ABSTRACT (maximum 200 words) Gallium Arsenide (GaAs) circuits are largely immune to slowly accumulated radiation doses and therefore do not need the shielding required by complimentary metal oxide semiconductor (CMOS) devices. This attribute renders GaAs circuits particularly attractive for space craft and military applications. However, it has been shown that GaAs circuits with short gate length transistors are excessively susceptible to single event upsets (SEU) due to enhanced charge collection at the edges of the gate called "edge effect". This thesis studies the SEU problem in two parts. Extensive computer modeling and simulation of a charged particle passing through various transistors of a low power, two-phase dynamic MESFET logic (TDFL) test chip was conducted using HSPICE in the first part. In the second part, new GaAs logic topologies are developed, simulated, and layed out in integrated circuits which require less power than directly coupled MESFET logic (DCFL) and should be less susceptible to single event upsets than TDFL circuits.				
14. SUBJECT TERMS Single Event Upset, Gallium Arsenide Logic			15. NUMBER OF PAGES 116	
			16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT UL	

NSN 7540-01-280-5500 Standard Form 298 (Rev. 2-89)

Prescribed by ANSI Std. Z39-18

Approved for public release; distribution is unlimited.

Radiation Tolerant, High Speed, Low Power  
Gallium Arsenide Logic

by

Kurt A. Wolfe  
Lieutenant, United States Navy  
B.S., United States Naval Academy, 1986

Submitted in partial fulfillment  
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL  
December 1993

Author:

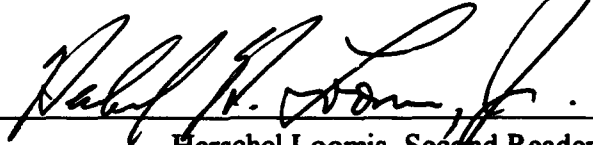


Kurt A. Wolfe

Approved by:



Douglas J. Fouts, Thesis Advisor



Herschel Loomis, Second Reader



Michael A. Morgan, Chairman  
Department of Electrical and Computer Engineering

## ABSTRACT

Gallium Arsenide (GaAs) circuits are largely immune to slowly accumulated radiation doses and therefore do not need the shielding required by complementary metal oxide semiconductor (CMOS) devices. This attribute renders GaAs circuits particularly attractive for space craft and military applications.

However, it has been shown that GaAs circuits with short gate lengths are excessively susceptible to single event upsets (SEU) due to enhanced charge collection at the edges of the gate called "edge effect".

This thesis studies the SEU problem in two parts. Extensive computer modeling and simulation of a charged particle passing through various transistors of a low power, two-phase dynamic metal semiconductor field effect transistor (MESFET) logic (TDFL) test chip is conducted using HSPICE in the first part. In the second part, new GaAs logic topologies are developed, simulated, and laid out on an integrated circuit which require less power than directly coupled MESFET logic (DCFL) and should be less susceptible to single event upsets than TDFL circuits.

Accession For	
NTIS	CRA&I <input checked="checked" type="checkbox"/>
DTIC	TAB <input type="checkbox"/>
Unannounced <input type="checkbox"/>	
Justification .....	
By .....	
Distribution /	
Availability Codes	
Dist	Avail and / or Special
A-1	

## TABLE OF CONTENTS

<b>I. Introduction .....</b>	<b>1</b>
<b>II. SEU Simulation Using HSPICE .....</b>	<b>7</b>
A. Background .....	7
B. Method and Results .....	8
<b>III. SEU Tolerant GaAs Circuits .....</b>	<b>13</b>
A. Psuedo-Complimentary MESFET Logic .....	13
1. PCML INVERTER .....	14
a. Determination of Noise Margins .....	15
2. PCML NOR Gate .....	18
B. Four Phase Dynamic MESFET Logic (FDML) .....	19
1. FDML Inverter .....	20
2. FDML NOR Gate .....	22
<b>IV. Integrated Circuit Layout .....</b>	<b>23</b>
A. PCML Circuits .....	24
B. DCFL Circuits .....	29
C. FDML Circuits .....	35
D. Completed Chip .....	39
<b>V. Comments and Conclusions .....</b>	<b>40</b>
A. SEU Simulation Using Hspice .....	40
B. New GaAs Circuits .....	40
C. Recommendations for Future Research .....	41
<b>Appendix A - SEU Simulations .....</b>	<b>42</b>
<b>Appendix B Chip Verification Simulations .....</b>	<b>80</b>
<b>References .....</b>	<b>110</b>

# I. INTRODUCTION

Gallium arsenide (GaAs) integrated circuits can operate at significantly higher frequencies than comparable circuits fabricated in silicon. GaAs circuits can also tolerate much higher total dose levels of ionizing radiation than silicon. (Approximately  $10^8$  rads for GaAs vs.  $10^6$  rads for CMOS) [Ref. 1, p. 126]

When exposed to ionizing radiation, a positive space charge develops in the insulating layers and along the Si-SiO<sub>2</sub> boundaries of a silicon device. This causes an increase in leakage currents and a shift in the gate threshold voltage levels of the device, which eventually results in device failure. [Ref. 1, p. 125] CMOS devices are particularly sensitive to this type of failure and therefore must be shielded when used in an area where radiation exposure can occur.

GaAs circuits are largely immune to these slowly accumulated radiation doses and therefore do not need the shielding required by CMOS devices. This attribute renders GaAs circuits particularly attractive for space craft and military applications. [Ref. 2]

However, it has been shown that GaAs circuits with short gate lengths (on the order of one micron) are excessively susceptible to single event upsets due to enhanced charge collection at the edges of the gate called "edge effect". [Ref. 3]

The single event upset phenomenon (SEU) is a transient error induced in an integrated circuit which arises from  $\alpha$ -particles, (protons), or heavy ions striking an individual cell or logic element. If in the vicinity of a transistor, the resulting charge

deposition can be sufficient to cause a deviation from its designed logic value which then causes a change of state in subsequent bistable circuitry. [Ref. 1, p. 127]

It is important to note that the continuing trend toward increased switching speeds, sub-micron device sizes, and decreased capacitance, increases the probability of a SEU in an integrated circuit. Understanding the behavior of charge dynamics in GaAs circuits subjected to ionizing radiation could lead to circuit topologies and system architectures that are less sensitive to SEUs.

Chapter II of this thesis will present the results of extensive computer modeling and simulation of a charged particle passing through various transistors of a low power, two-phase dynamic FET logic test chip. Results of the simulations will then be compared to picosecond-laser induced charge collection measurements taken at various points in the circuit. The purpose of the simulations was to provide a benchmark which could be used for further GaAs circuit development. Using the computer simulations, SEU tolerance could be estimated, allowing various circuit layouts and modifications to be evaluated prior to submitting the design for fabrication.

In addition to SEU susceptibility, static GaAs circuits such as direct-coupled FET logic (DCFL) present the problem of excessive power consumption, typically 0.5 mW/gate. [Ref. 4] VLSI (very large scale integration) implementation of GaAs circuits is therefore limited in part by the number of gates that can be included on chip while operating within an acceptable temperature range.

The primary explanation for the power dissipation problem in GaAs circuits is the fact that p-channel FETs are not used as pull-up transistors as they are in CMOS circuits because they are much slower than GaAs nfets. Parasitic capacitance also plays a major role in power dissipation at high frequencies. However, since the dielectric constant of the undoped GaAs substrate is very low, and because it is semi-insulating, parasitic capacitance does not play as great a role in power dissipation as it does in most CMOS devices. (see Figure 1) [Ref. 5]

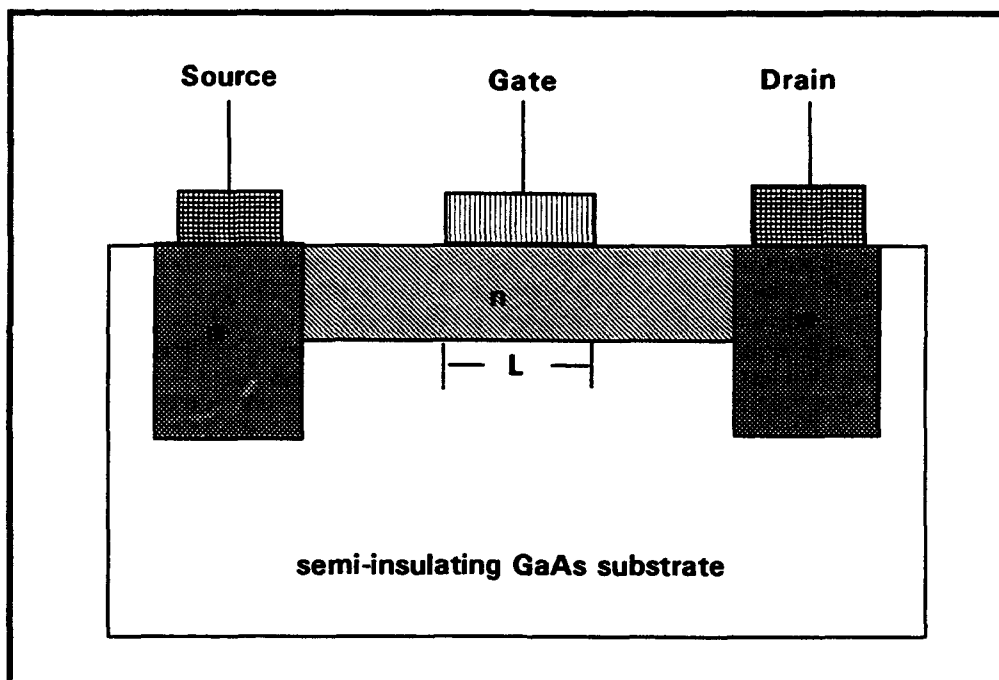


Figure 1 MESFET Cross-section

The cross-section of a typical GaAs n-type MESFET is shown in Figure 1. The gate is composed of Schottky barrier metal and is laid directly over the active region of the transistor. The channel of an enhancement mode MESFET is normally "off" and requires a positive voltage to be applied to the gate for channel conduction to occur. Depletion



mode MESFETS, on the other hand, are normally "on" and require a negative gate voltage in order to turn them "off". The amount of current that flows through the channel (marked with an "n" in figure one in reference to its moderate doping level) when there is a voltage differential between the drain and source depends upon the amount of voltage applied to the gate in addition to the length ("L" in Figure 1) and width of the gate itself.

The lack of a fast pull-up transistor with an opposite gate threshold voltage to that of the pull-down nfet transistor precludes the implementation of a complimentary GaAs MESFET logic circuit with low static power dissipation. In order to present a "low" logic output to a succeeding gate, one commonly used logic family called "directly coupled MESFET logic" (DCFL) employs circuits which dissipate power by sinking current for the duration of the "low" output state.

With this in mind, efforts to develop GaAs circuits with a low static power consumption have led to a new family of logic called "two-phase dynamic FET logic" (TDFL) which achieves its result through the use of non-overlapping clocks. [Ref. 4]

Typical operation of a TDFL inverter is as follows. (Refer to Figure 2) One phase of the negative valued clock is used to turn on a depletion mode transistor whose drain is attached to Vdd and source is attached to the output node, causing a charge to be stored on the output node of the inverter. At the same time, the input value is passed through a clocked dfet to the gate of an enhancement mode fet. A third dfet is attached between the output node and the drain of the enhancement mode fet whose source is attached to ground. The second phase of the clock is applied to the gate of the third dfet which

discharges the output node to "0" if the input was a "1". If the input was a "0" the enhancement mode FET remains off and the output node remains charged at "1"

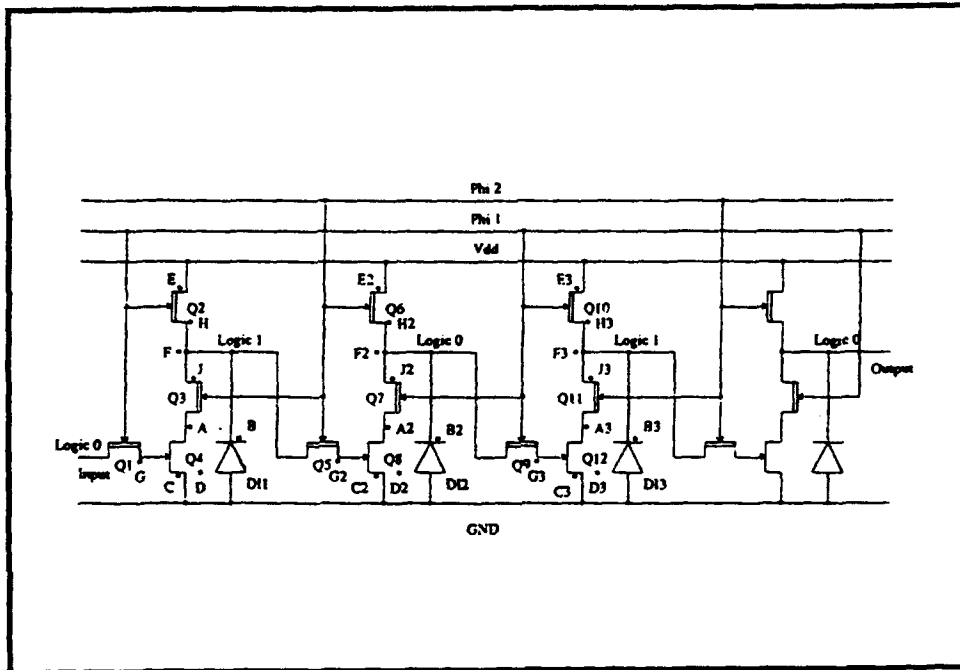


Figure 2 Schematic Diagram of TDFL Test Structure

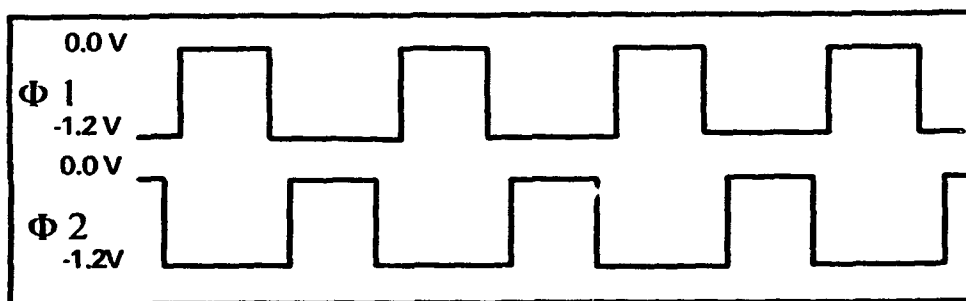


Figure 3 Non-overlapping Two-phase Clock

The TDFL family of logic was the subject of the testing and computer simulation discussed in chapter two. There it is shown that, while TDFL requires a very low power budget compared to other GaAs logic families, it too suffers from a high susceptibility to

SEUs. Chapter III presents alternative circuit designs which attempt to exploit the knowledge gained from the SEU testing discussed in Chapter II. The viability of the new circuits was tested using HSPICE [Ref. 6]. Balanced noise margins were then achieved in the new logic gates by adjusting the gate lengths and widths of the various transistors used.

Chapter IV illustrates the design layout of the experimental chip. The layout was verified using HSPICE to complete a pad-to-pad simulation of each device.

Finally, in Chapter V, comments and conclusions are discussed and recommendations for further research are presented.

## II. SEU SIMULATION USING HSPICE

### A. BACKGROUND

Gallium Arsenide, a III-V compound semiconductor, derives its properties from the third and fifth columns of the periodic table. The major physical characteristic that makes its use attractive in integrated circuit fabrication is the speed at which electrons move within the semiconductor. Electron mobility in n-type GaAs is up to ten times that of silicon. [Ref. 5]

Another significant benefit of fabricating integrated circuits in GaAs is their inherent tolerance to total dose radiation. [Ref. 1] Space craft and military devices must operate reliably in this type of an environment for long periods of time, and could therefore benefit from this intrinsic radiation hard quality through reduced shielding costs and increased life expectancy of onboard electronics.

Although GaAs devices have a much higher total dose tolerance than silicon devices, when they are exposed to ionizing radiation, a reliability problem is introduced. The problem manifests itself in the form of a single event upset (SEU). As circuit dimensions are reduced, the SEU problem is amplified. [Ref. 2]

Previous research involved firing a laser into GaAs dynamic logic circuits to induce SEUs. The purpose of this portion of the research was to gather data which could be used to develop SEU tolerant GaAs systems. Extensive evaluation of a test chip composed of Two-Phase Dynamic Logic (TDFL) structures was completed using the laser testing

method and the data was used as a basis for comparison in the computer modeling and simulation discussed in this report. [Ref. 7, 8]

The cost of developing a SEU tolerant gallium arsenide integrated circuit could be greatly reduced in terms of time as well as money if the design could be modeled on a computer to determine SEU sensitivity prior to fabrication. For this reason HSPICE, the circuit simulation software package used to develop the chip which was used in the laser testing was chosen to attempt simulation of SEUs in GaAs logic circuits [Ref. 6].

An ionizing particle creates electron-hole pairs when it penetrates the substrate of a GaAs I.C. The charge which results can be modeled as a current source that takes approximately 5 picoseconds to reach its maximum, after which it decays exponentially to near zero in approximately 250 picoseconds. [Ref. 7] An example of the pulsed, exponential current source used in the HSPICE simulations is shown in Figure 4.

## **B. METHOD AND RESULTS**

A circuit description file was created for the TDFL test chip which was used in the laser testing phase. A current source similar to that in Figure 4 was connected across each transistor in the circuit. The four separate current source configurations tested for each transistor consisted of connections between the gate and source, the gate and drain, the source and drain, and the gate and substrate.

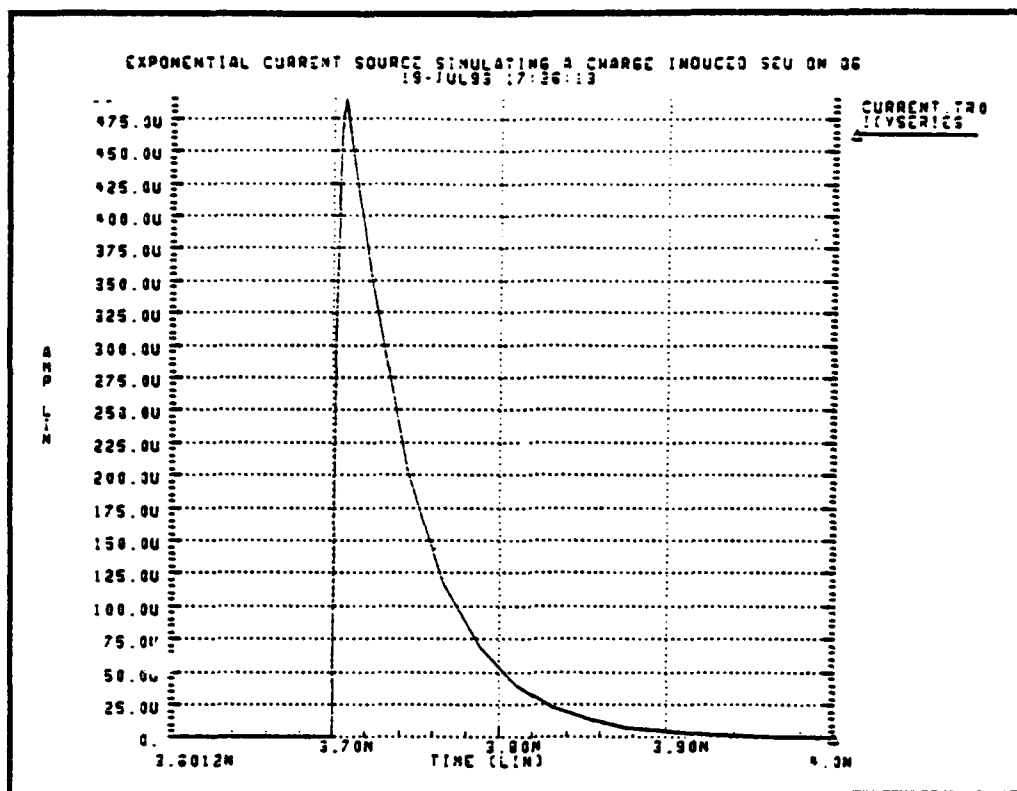


Figure 4 Pulsed Exponential Current Source

In the cases where a single event upset could be modeled, the minimum amount of current required to induce the event was determined by iteratively decreasing the pulse magnitude until it reached a threshold value. A second factor in the simulation of the SEU, pulse timing, was also considered.

Since TDFL relies upon clock signals to transfer charge from node to node, the timing of the current pulse used to simulate the SEU was critical. The most sensitive point for the current pulse to occur, relative to the inverter clocks, was therefore determined by performing iterative simulations for each event.

Figure 5 shows a simulation of a single event upset of transistor Q3 with the inducing current source attached to its source and drain. The input was held at a constant

0.6 volts which represents logic "1". The non-overlapping clocks are included as a timing reference. The reference for a reliable "0" logic value for the simulations was considered to be less than 0.1 volts. A reliable "1" was considered to be greater than 0.4 volts. Voltage outputs between 0.1 and 0.4 volts were considered metastable voltages that could not be recognized reliably as a "0" or a "1" in the presence of noise by subsequent logic gates in the circuit.

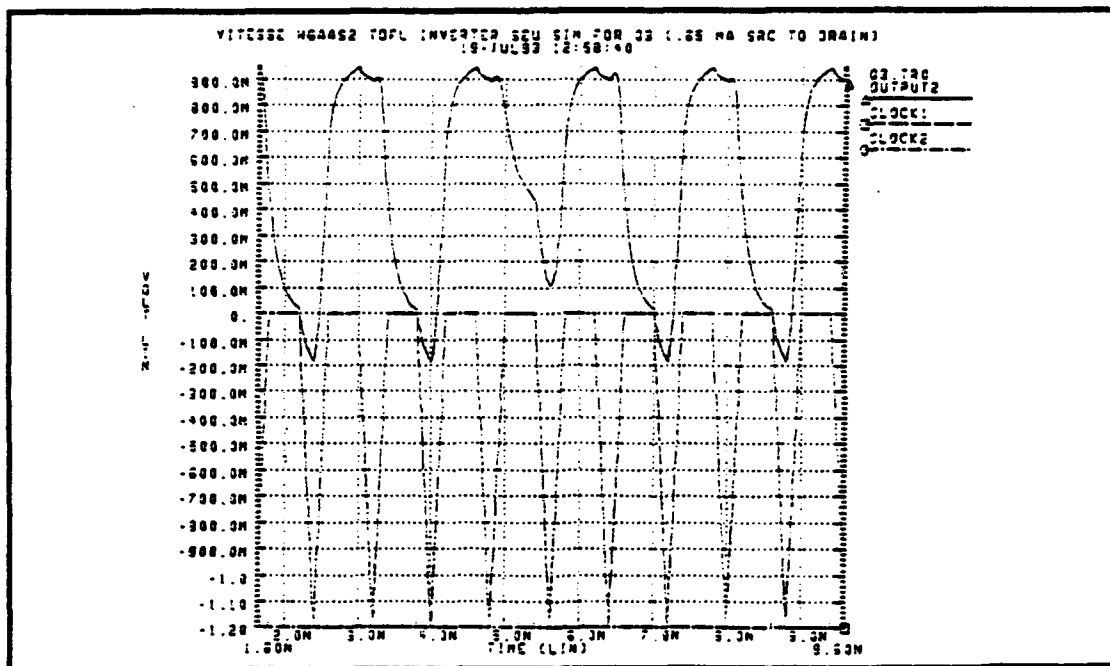


Figure 5 SEU of Transistor Q3

Upon determination of the most sensitive timing and minimum amount of current required to precipitate a single event upset in each transistor, the total charge required to generate the SEU was calculated.

This was accomplished by using HSPICE to simulate the same current source attached to an ideal capacitor. The asymptotic voltage limit of the charging capacitor indicated the magnitude of the charge. ( $Q = CV$ ) Figure 6 shows a comparison of the

amount of charge required to generate an SEU with the current source connected to the gate and drain (top curve) and then connected to the source and drain. (lower curve) This is an indication of the fact that the exact point of impact of an ion with the transistor is as critical as the amount of charge it deposits.

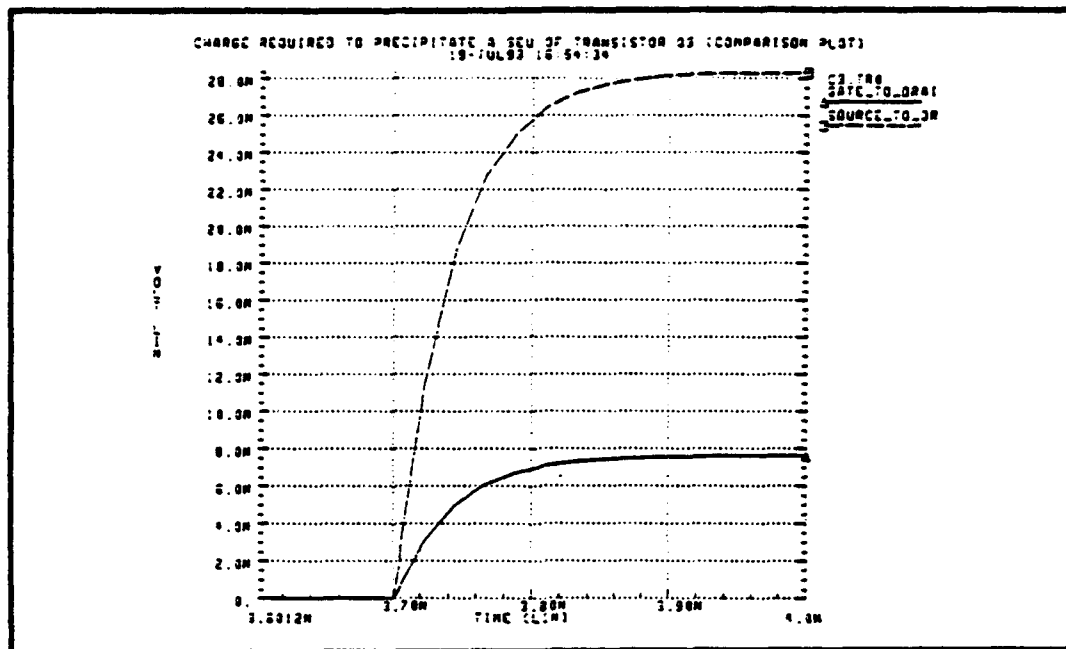


Figure 6 Charge required to Precipitate a SEU of Q3



Results of all of the simulations are shown in Table 1. Entries denoted by " \*\*\* " indicate a configuration that did not produce a simulated SEU in HSPICE.

**TABLE 1 SIMULATED CHARGE REQUIRED TO PRECIPITATE A SEU**

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
Source - Drain	1.30	6.54	28.40	7.85	4.66	23.96	108.90	32.30
Gate - Source	**	**	7.65	2,180.00	9.05	**	34.70	3.71
Gate - Drain	1.30	6.54	7.65	4.80	3.71	23.96	108.90	3.00
Gate - Bulk	**	**	**	2,180.00	**	**	**	3.71
Charge in femtocoulombs. ** = No simulation for indicated configuration								

The experimental data obtained through laser testing is shown in Table 2. The letters correspond to the locations on the TDFL test chip of Figure 2 that were subjected to laser testing.

**TABLE 2 LASER INDUCED SEU RESULTS**

	G	E	J	C	G2	E2	J2	C2
Charge	54.20	37.60	20.90	30.00	20.90	100.10	**	15.00
Charge in femtocoulombs. ** = Could Not Cause a SEU								

The data presented thus far indicates that TDFL circuits are highly susceptible to SEUs. In the following chapter, two experimental logic topologies are introduced which should be less sensitive to SEUs. The methods employed to affect this decreased sensitivity include the reduction in the number of transistors required to implement a logic function and a decreased emphasis on charge sharing.

### **III. SEU TOLERANT GAAS CIRCUITS**

#### **A. PSUEDO-COMPLIMENTARY MESFET LOGIC**

The charge build up on the critical nodes of a GaAs circuit due to ionizing radiation is the underlying cause of single event upsets. If the majority of the energy imparted to a circuit by a potential SEU could be absorbed by the power source driving the logic gate, it would be reasonable to assume that the event would have a much smaller effect on the design performance of the circuit.

A new family of logic called Pseudo-Complimentary MESFET Logic (PCML) is introduced here in which the output does not depend upon clocks to shift a stored charge from one node to another as in TDFL. It consists of an all EFET design with complimentary output nodes, either pulled all the way to the power rail or all the way to ground by a transistor that is always turned on and operating in the saturation region with a low channel resistance. This direct path to the designed logic value provides a means of shunting charge imparted to the device by a potential SEU. Also, the transistors that are turned off are completely cut off. Individual logic gates, their design specifications, and theory of operation are described. All of the standard logic functions (not, nand, nor) can be constructed in this family. The operation of PCML gates is similar to that of silicon CMOS in that there is no static flow of current from the power rail to ground. Power only flows when the logic gate is changing states, greatly reducing total power consumption

over DCFL circuits. The inputs and outputs are also directly compatible with existing TDFL and DCFL logic and the power rails are compatible with those of low voltage silicon CMOS.

## 1. PCML INVERTER

The PCML inverter consists of four enhancement mode FETs. (see Figure 7)

In order to create the inverter, two transistors are attached in series. The remaining source and drain are then attached to power and ground respectively. Complimentary inputs are attached to the gate nodes and the output is taken from the shared node of the transistor pair. The remaining two transistors are configured in a similar manner, with the gate inputs attached in opposite order. This yields a complimentary output to that of the first transistor pair.

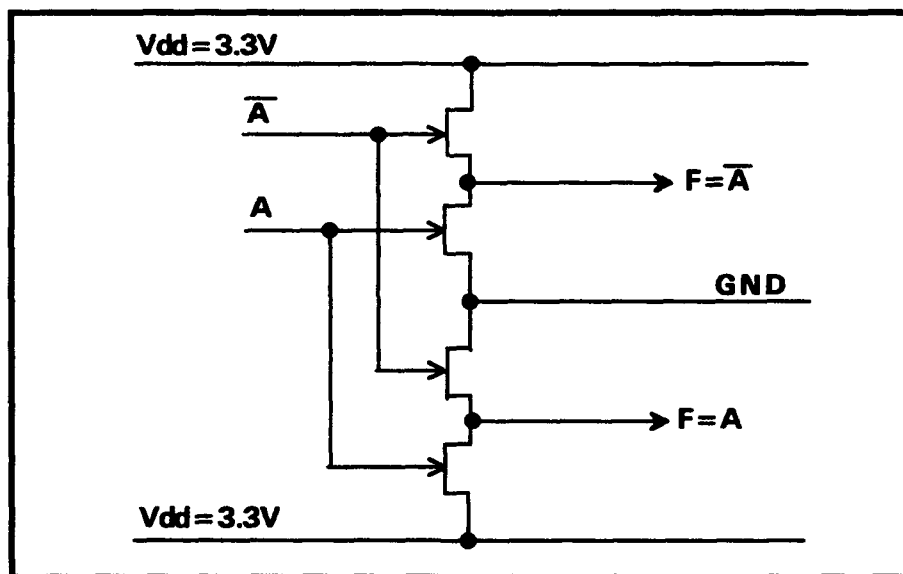


Figure 7 PCML Inverter

The total voltage swing at the gate of the enhancement mode GaAs MESFETs used in PCML is restricted to values between 0.0 volts and 0.6 volts. Due to the small variation between its high and low values, very little room for error is afforded in terms of translating a gate voltage to its corresponding binary logic value. It is therefore desirable to have the output of a logic gate operate symmetrically around the median value of 0.3 volts. Achieving this result is called balancing the noise margins. It maximizes the noise tolerance of the logic circuit and was considered an important factor in developing the PCML family of circuits.

#### *a. Determination of Noise Margins*

The noise margins of a logic gate are parameters which define the amount of noise voltage that can be tolerated at the input of a logic gate without affecting its output. These parameters are divided into the low noise margin,  $NM_L$ , and the high noise margin,  $NM_H$ . [Ref. 9]

The low noise margin is defined as the voltage difference between the maximum voltage of a driving gate's low output ( $V_{OLmax}$ ) and the maximum voltage that the input of the following gate will recognize as a low input ( $V_{ILmax}$ ).

$$NM_L = | V_{ILmax} - V_{OLmax} |$$

The high noise margin is defined as the voltage difference between the minimum voltage of a driving gate's high output ( $V_{OHmin}$ ) and the minimum voltage that the input of the following gate will recognize as a high input ( $V_{IHmin}$ ).

$$NM_H = | V_{OHmin} - V_{IHmin} |$$

GaAs circuits are restricted to a maximum voltage at the input of a gate of approximately 0.6 volts. At approximately 0.6 volts, the Schottky barrier diode created at the gate of the transistor begins to conduct heavily. This limitation precludes improved noise immunity from being achieved by operating the device at higher voltages. A further increase in gate voltage above 0.6 volts does not result in a significant increase in current conduction through the channel of the transistor, and in fact only contributes to the problem of power dissipation already inherent in GaAs circuits.

With GaAs EFETs, as with most low voltage integrated circuits, a relatively small amount of noise can cause a transistor to inadvertently turn on or off. This sensitivity magnifies the importance of closely balanced noise margins. The only part of the fabrication process that can be altered by the design engineer that will effect the noise margins is varying the size ratios of the pull-up and pull down transistors.

Multiple iterations were performed using HSPICE in order to determine the transistor size ratio which would provide the best DC transfer characteristics in terms of balanced noise margins for PCML gates. It was found that the most appropriate ratio for

the gate dimensions of the pull-up transistor to that of the pull-down transistor for a PCML logic gate is 12:1.

Figure 8 shows the DC transfer characteristic of a PCML inverter with a four inverter load on its output. The straight line represents a voltage source ramping from an initial value of 0.0 volts to a final value of 0.6 volts. The curved line shows the output of the inverter shifting as expected from 0.6 volts to 0.0 volts as the input ramps up. It can be seen that the noise margins are very closely balanced by noting that the two curves cross near 0.3 volts.

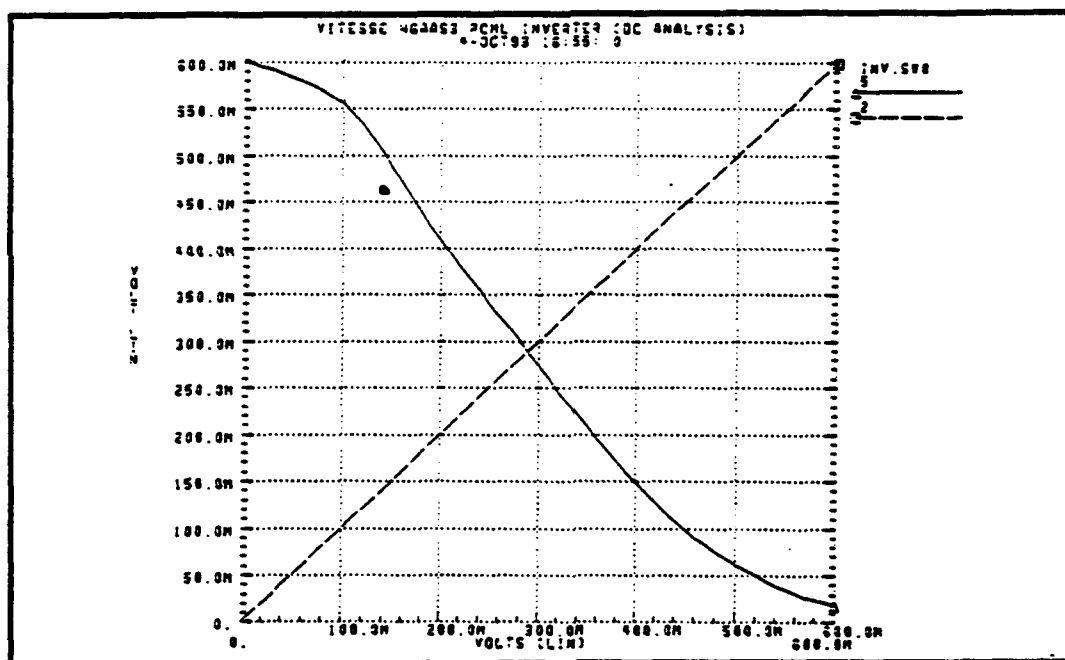


Figure 8 DC Transfer Characteristic of a PCML Inverter

Transient analysis of a DCFL inverter yielded an average delay time of 133 picoseconds. The transient analysis of the circuit, shown in Figure 9, illustrates the rise and fall times of the complimentary outputs of the PCML inverter.

From Figure 9, average delay time of the PCML inverter is:

$$T_{av} = [t_r + t_f]/4 = [235\text{E-}12 + 195\text{E-}12]/4 = 108\text{E-}12 \text{ seconds}$$

This is a twenty-three percent increase in speed over the DCFL inverter.

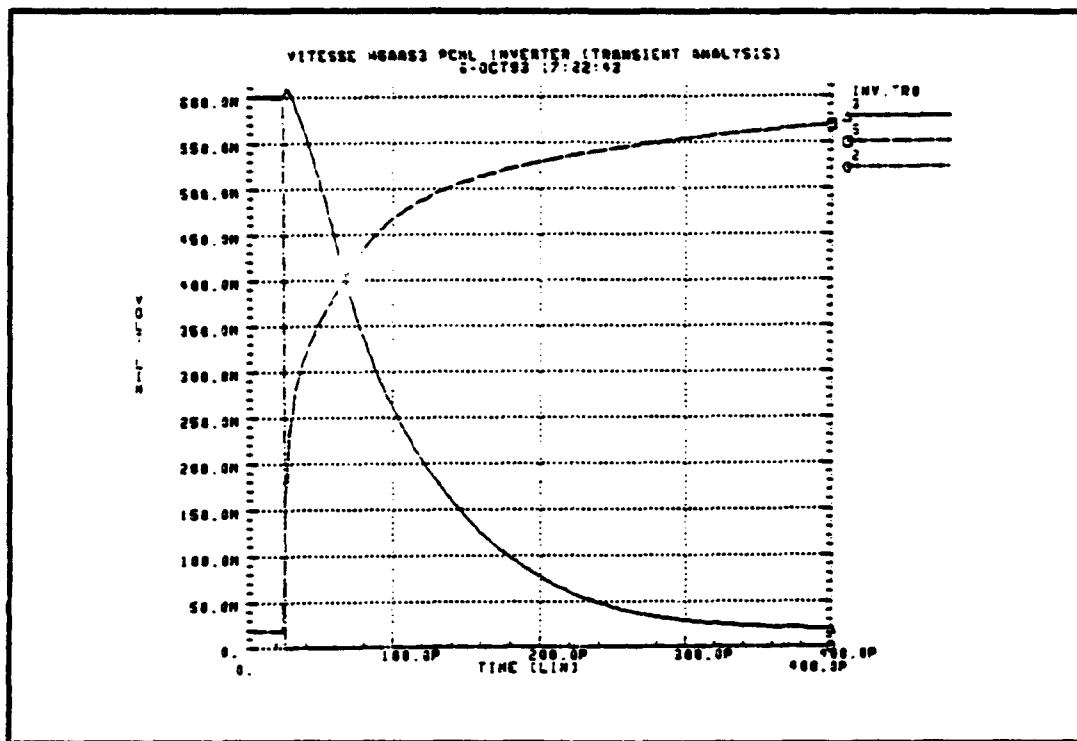


Figure 9 Transient Analysis of PCML Inverter

## 2. PCML NOR Gate

A schematic diagram of the PCML nor gate is shown in Figure 10. As in the case of the inverter, complimentary outputs are generated which can be used to detect the occurrence of a SEU by the use of a simple XOR gate. Operation of the logic gate is similar to that of the inverter described above. The complimentary inputs are used to turn on enhancement mode transistors which pull the output node completely to the ground or the power rail. The average delay time of the gate is 288 picoseconds.

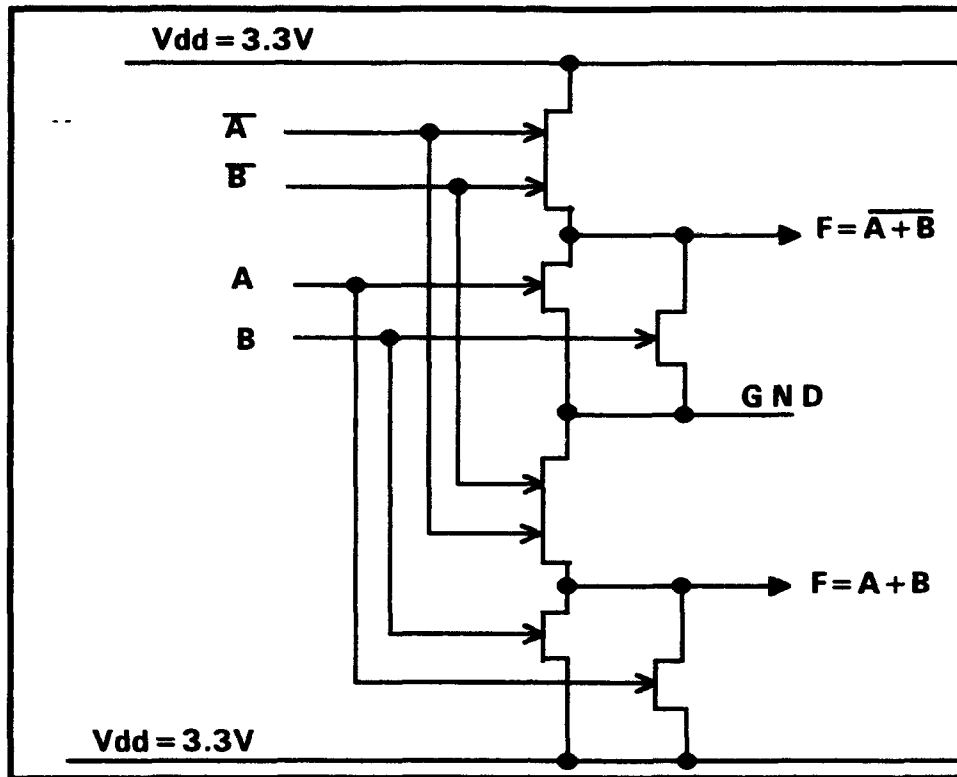


Figure 10 PCML NOR Gate

## B. FOUR PHASE DYNAMIC MESFET LOGIC (FDML)

Four phase dynamic MESFET logic (FDML) is similar to TDFL in that it is a ratioless logic family which depends upon non-overlapping clock signals to shift charge from node to node. The two main advantages of FDML over TDFL circuits are the elimination of the pass transistor from the gate inputs and the generation of complimentary outputs. The elimination of the pass transistor reduces the total number of transistors required to generate complimentary outputs, thereby reducing the probability of a SEU.



The complimentary outputs enable the detection of a SEU through the use of an XOR gate. The major disadvantages of FDML to TDFL are the use of a four phase clock and the extra area required to route the complimentary inputs.

### 1. FDML Inverter

The FDML inverter consists of six transistors and two diodes. (see Figure 11)

The diodes are used to add capacitance to the output nodes of the gate in order to improve its low frequency operation. Increasing the size of the diodes decreases the speed of the circuit.

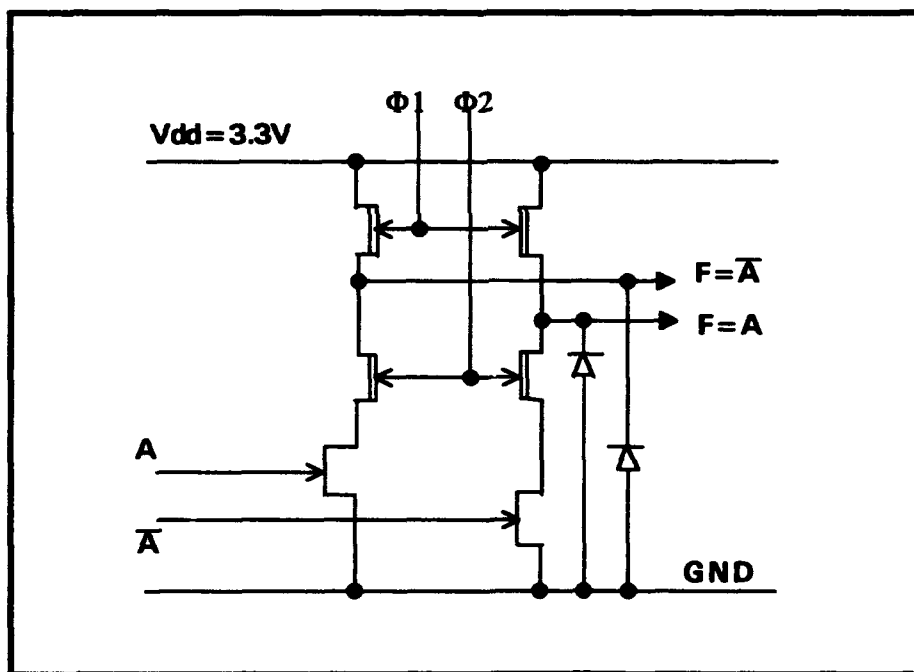


Figure 11 FDML Inverter

The output of an FDML inverter with the complimentary inputs held constant is shown in Figure 12. Only two of the four clock phases are shown for purposes of clarity.

Notice that both nodes charge to a logic value "1" while phase one of the clock is high. When phase two of the clock goes high the charges stored on the output nodes assume the opposite value of their respective inputs. A subsequent FDML gate would employ clock phases three and four.

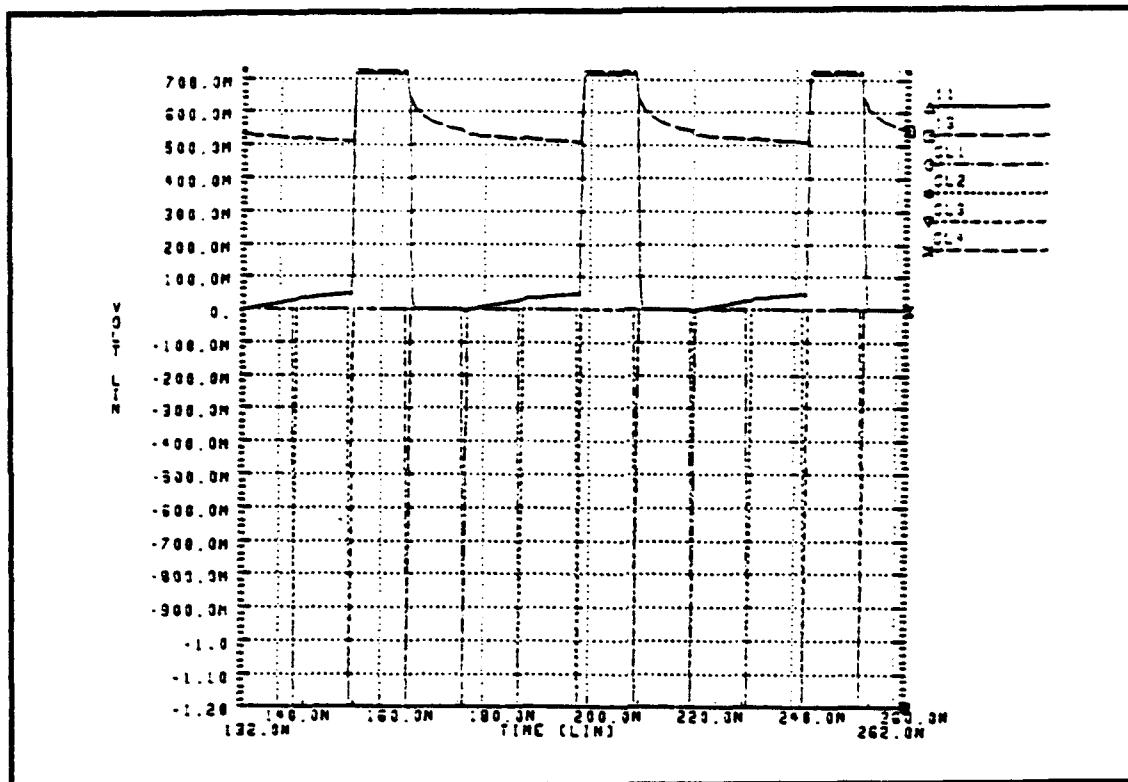


Figure 12 FDML Inverter Output - Inputs Held Constant

## 2. FDML NOR Gate

The circuit shown in Figure 13 is a FDML NOR gate. The clock phases are employed in the same manner as those in the inverter of Figure 11.

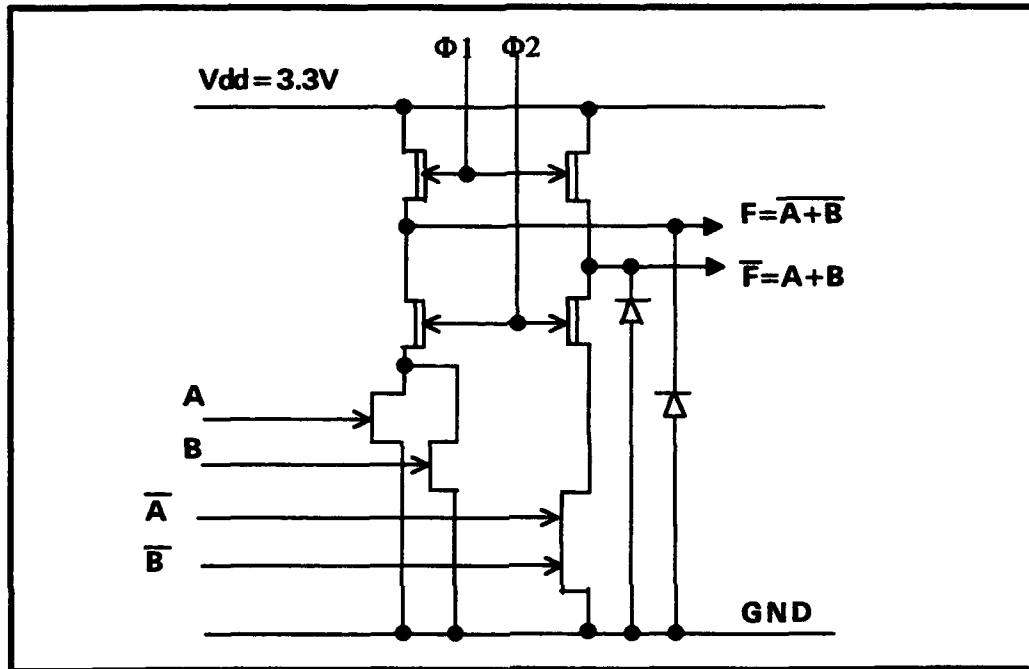


Figure 13 FDML NOR Gate

The simulations of the circuits discussed in this chapter illustrate the viability of their design. Chapter IV illustrates the implementation of the experimental topologies on an integrated circuit.

## **IV. INTEGRATED CIRCUIT LAYOUT**

To further characterize and test the operation of the PCML and FDML circuits, a test and evaluation integrated circuit was designed. In addition to the circuits shown in the previous chapter, several other test structures were placed on the chip. The additional circuits include DCFL circuits which implement the same logic as a means of comparison for the PCML and FDML test structures.

A hierarchical approach was used to accomplish the actual layout of the experimental integrated circuit to be fabricated. Individual gates were laid out and extracted using MAGIC, and simulated using HSPICE to verify proper construction. [Ref. 10] After all individual gate design was completed, the test circuits for each family of logic were laid out by importing multiple instances of the basic gates and laying the interconnect between them in the appropriate manner.

Following the layout and extraction of the test circuits, HSPICE was again used to check the circuit for design errors. Finally, the test circuits were connected to their respective input receivers, output drivers and pads. A final HSPICE simulation was done from input pads to output pads for all circuits to assure proper layout and design prior to submitting the chip design to Vitesse Semiconductor for fabrication via the MOSIS service.

## A. PCML CIRCUITS

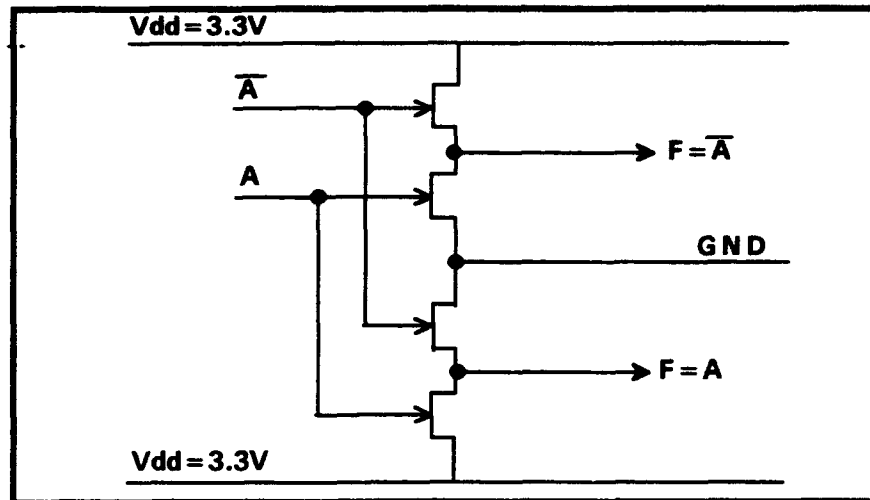


Figure 14 PCML Inverter Schematic

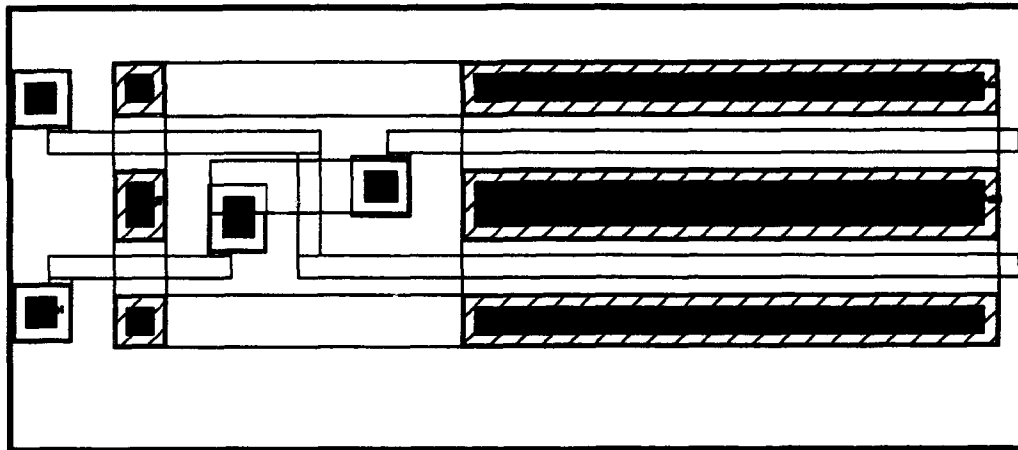


Figure 15 PCML Inverter Layout

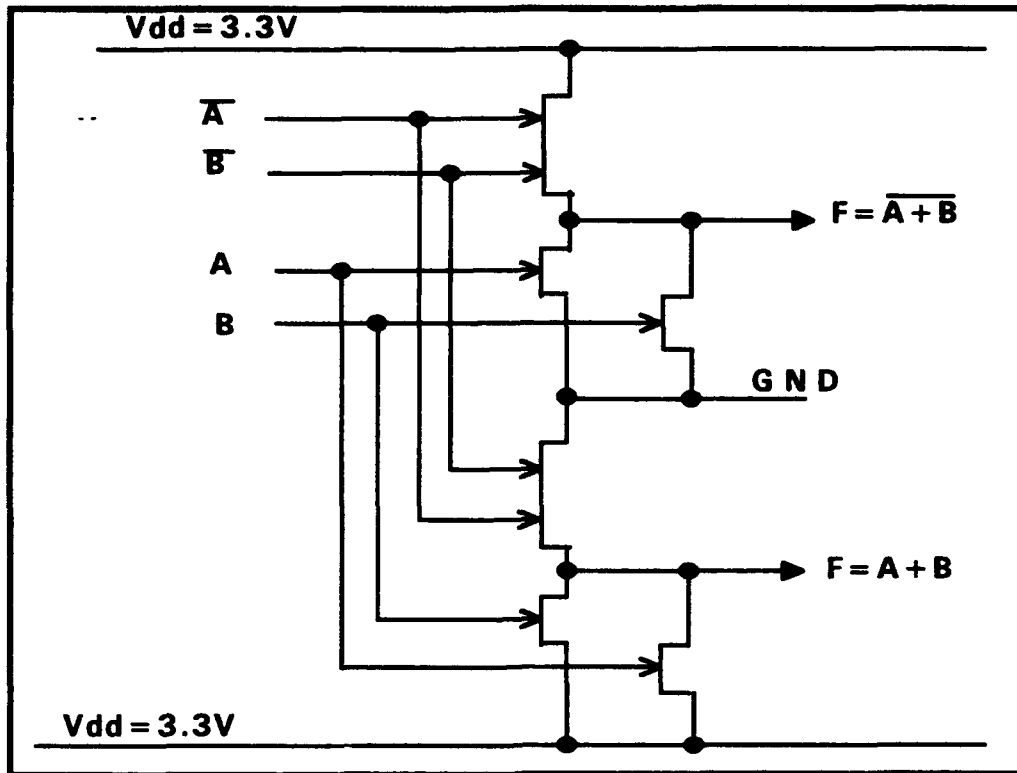


Figure 16 PCML Nor Gate Schematic

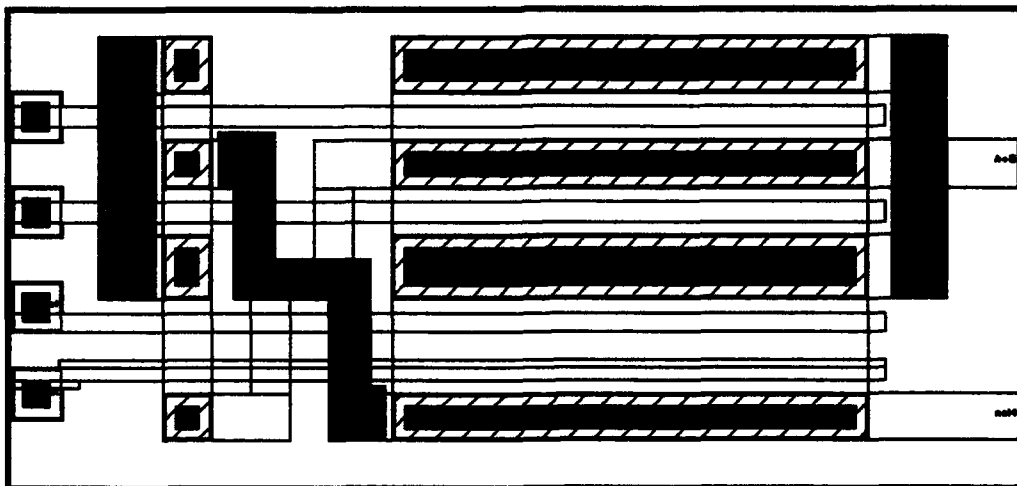


Figure 17 PCML NOR Gate Layout

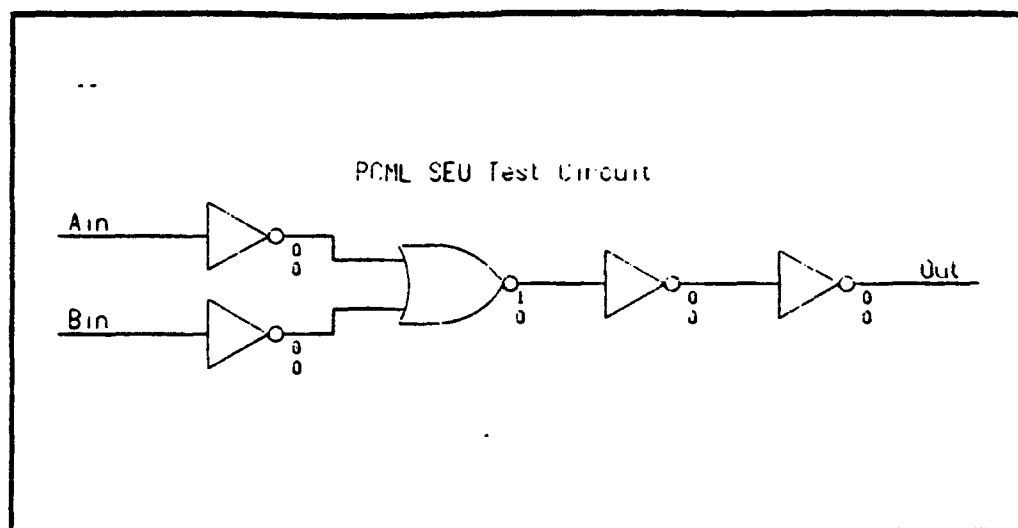


Figure 18 PCML SEU Test Circuit Schematic

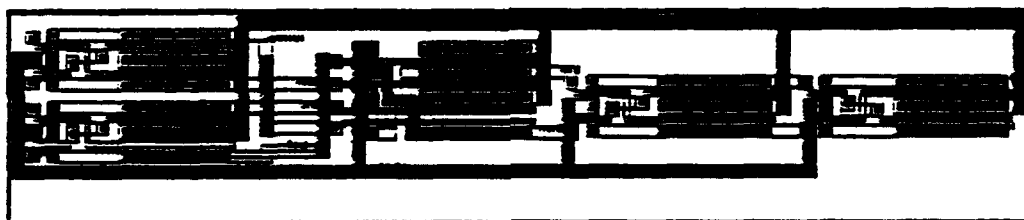


Figure 19 PCML SEU Test Circuit Layout

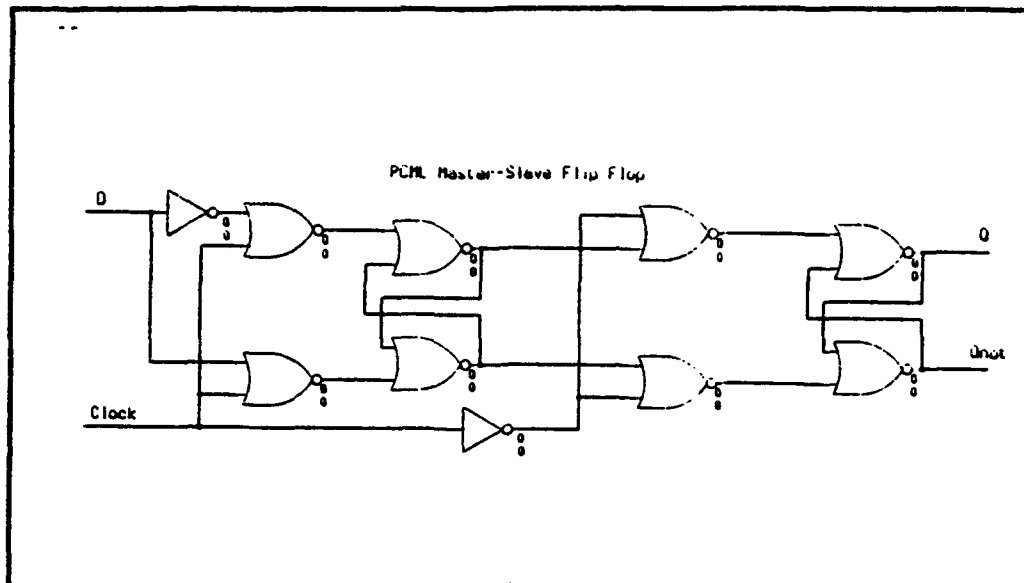


Figure 20 PCML Master-Slave Flip-Flop Schematic

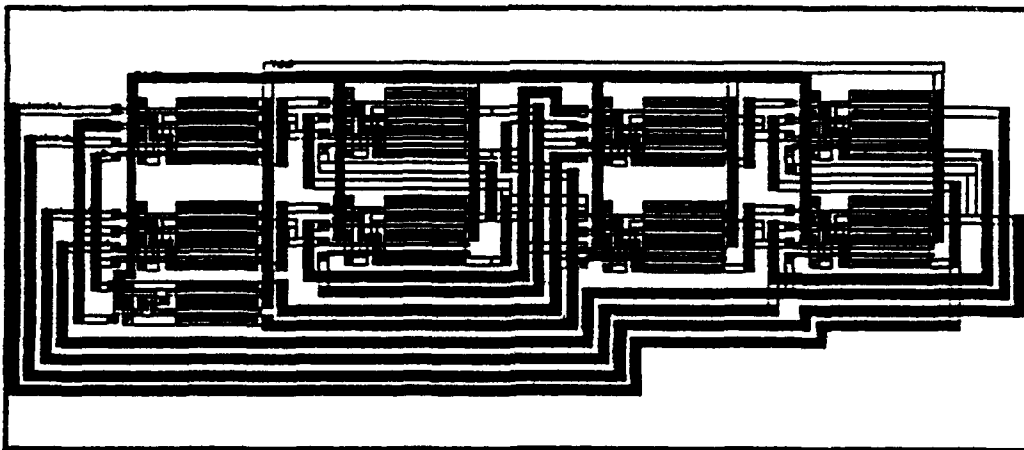


Figure 21 PCML Master-Slave Flip-Flop Layout

The PCML ring oscillator shown in Figure 23 will be used to verify the simulated speed of PCML logic. Since the usable voltage swing at the gate of the enhancement mode transistors used in PCML is only 0.0 volts- 0.6 volts, the voltage used on the power rails could conceivably be reduced without affecting the output logic. One test to be



performed using the circuit will be to plot the maximum operating frequency of PCML as the rail voltage is reduced. An advantage of lowering the rail voltage is a reduction in the power dissipation of the circuit. The speed of the circuit should not be significantly reduced as a result of the lowering the power rail voltage.

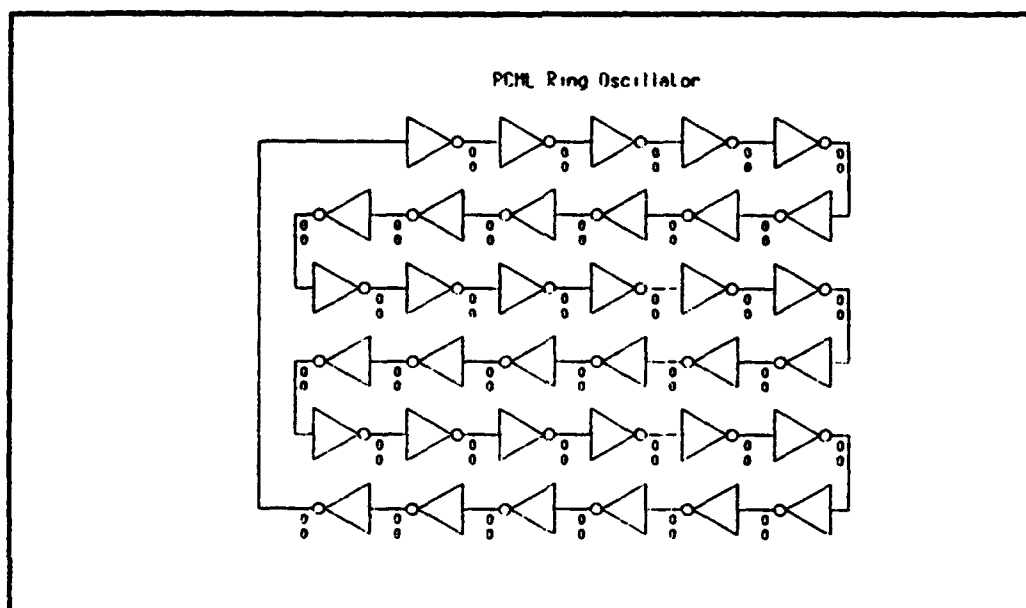


Figure 22 PCML Ring Oscillator Schematic

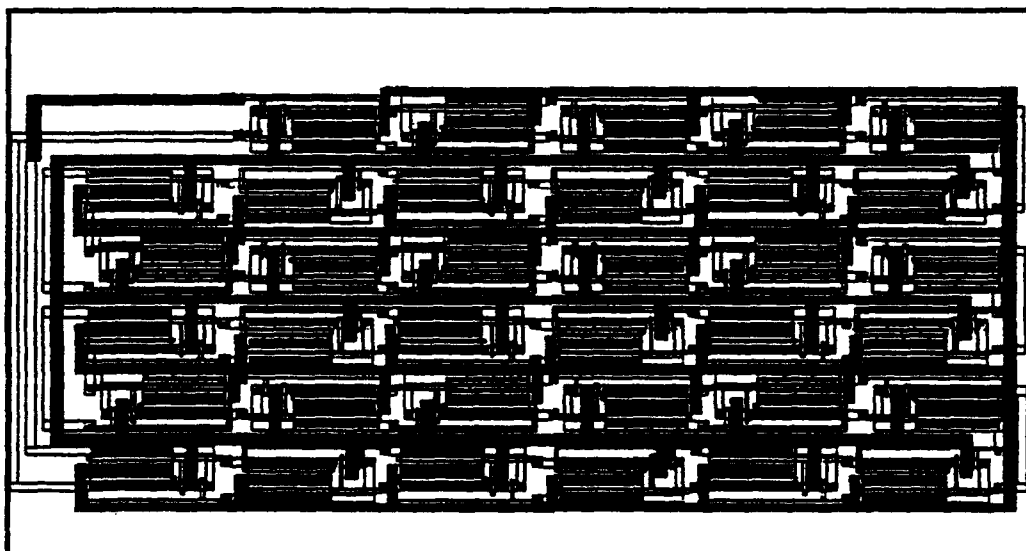


Figure 23 PCML Ring Oscillator Layout

## B. DCFL CIRCUITS

DCFL test circuits shown here were included on the final layout of the chip so that a basis of comparison, in terms of speed and power consumption, could be established using an identical fabrication process to that used for PCML and FDMML.

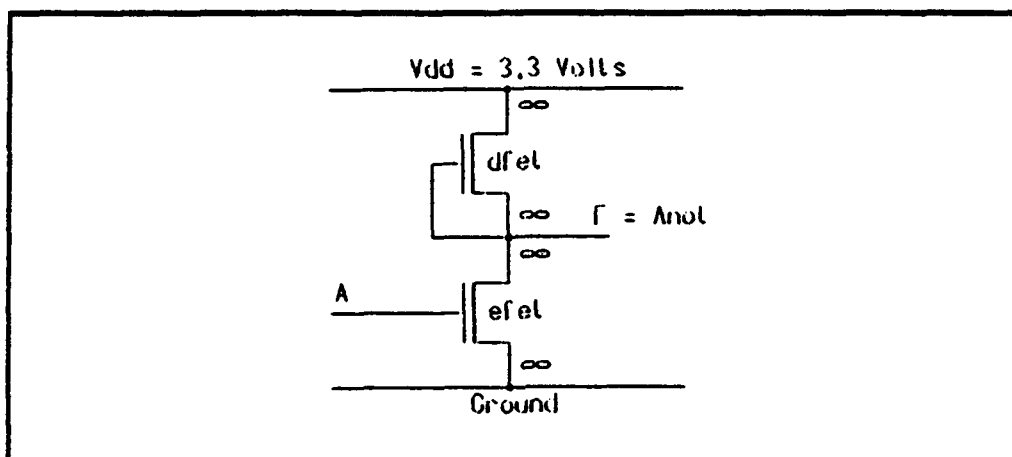


Figure 24 DCFL Inverter Schematic

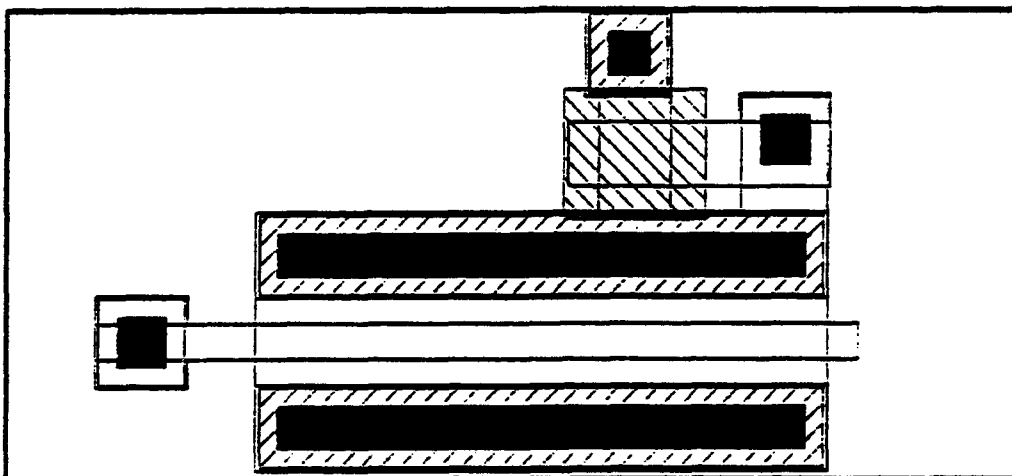


Figure 25 DCFL Inverter Layout

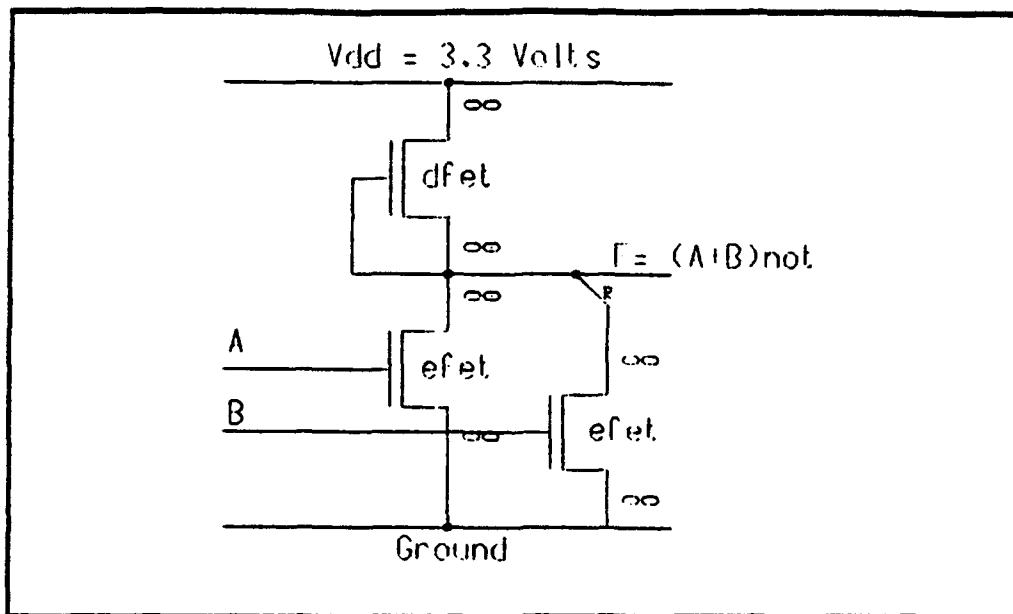


Figure 26 DCFL NOR Gate Schematic

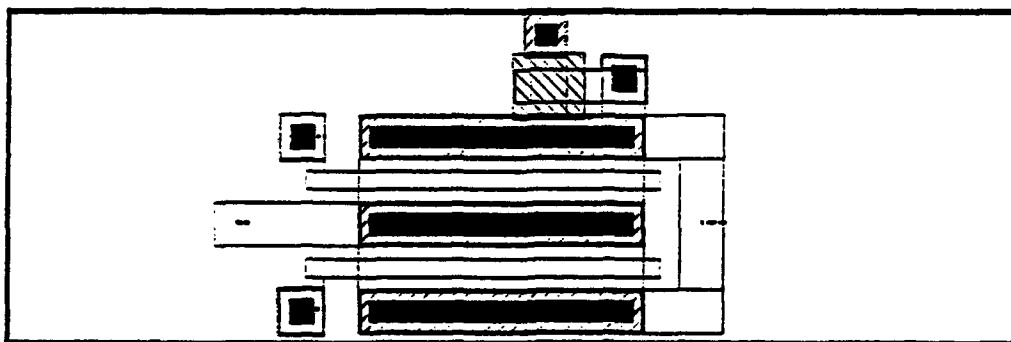


Figure 27 DCFL NOR Gate Layout

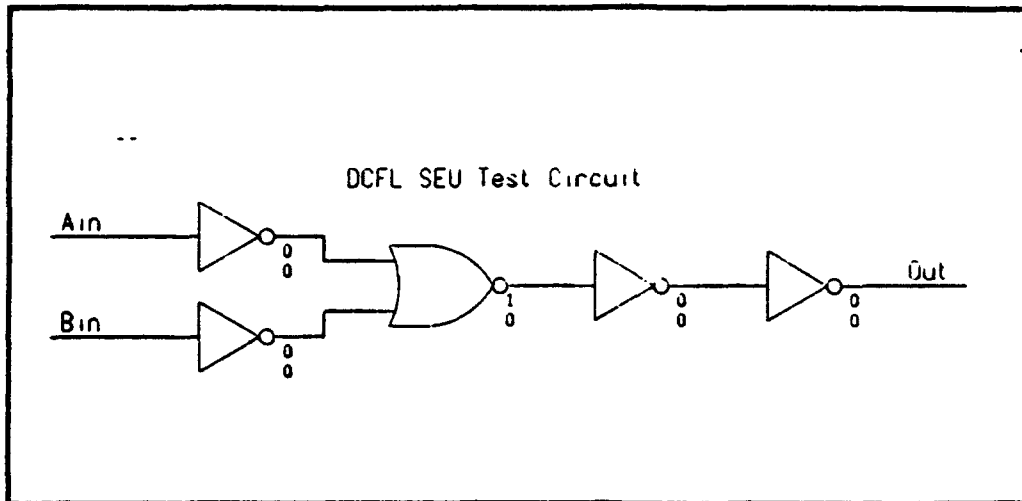


Figure 28 DCFL SEU Test Circuit Schematic

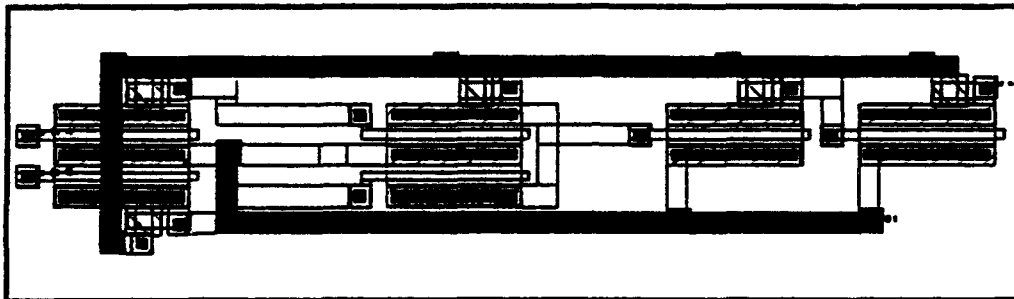


Figure 29 DCFL SEU Test Circuit Layout

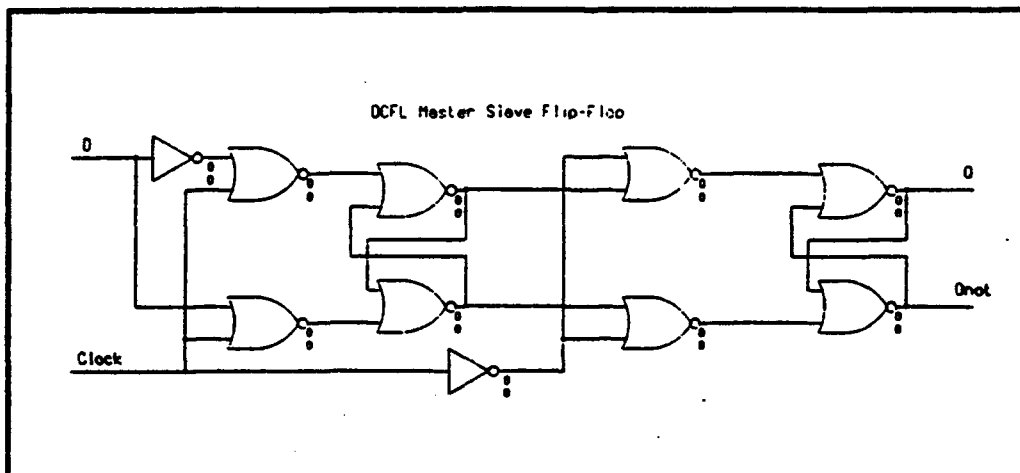


Figure 30 DCFL Master-Slave Flip-Flop Schematic

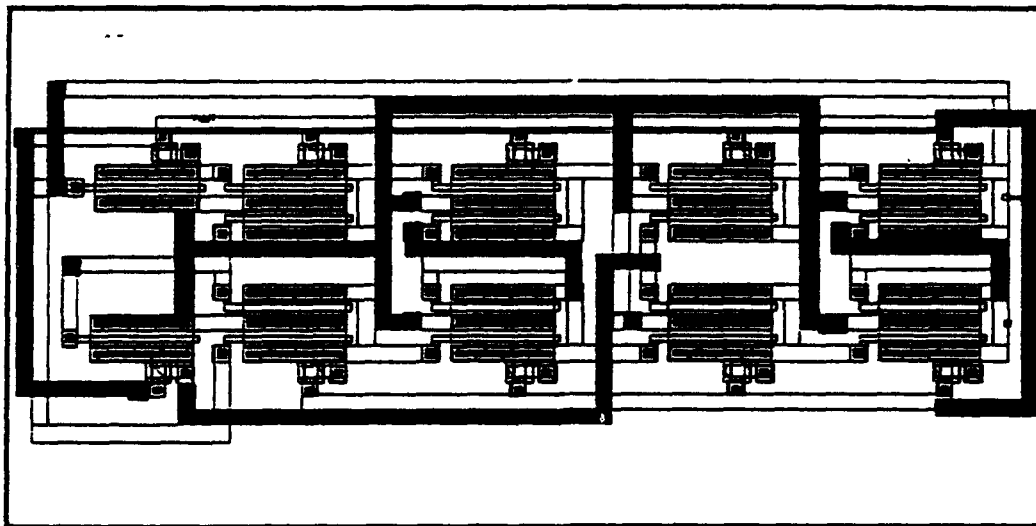


Figure 31 DCFL Master-Slave Flip-Flop Layout

The DCFL ring oscillator layout shown in Figure 33 will be used to compare the logic speed of DCFL to that of PCML.

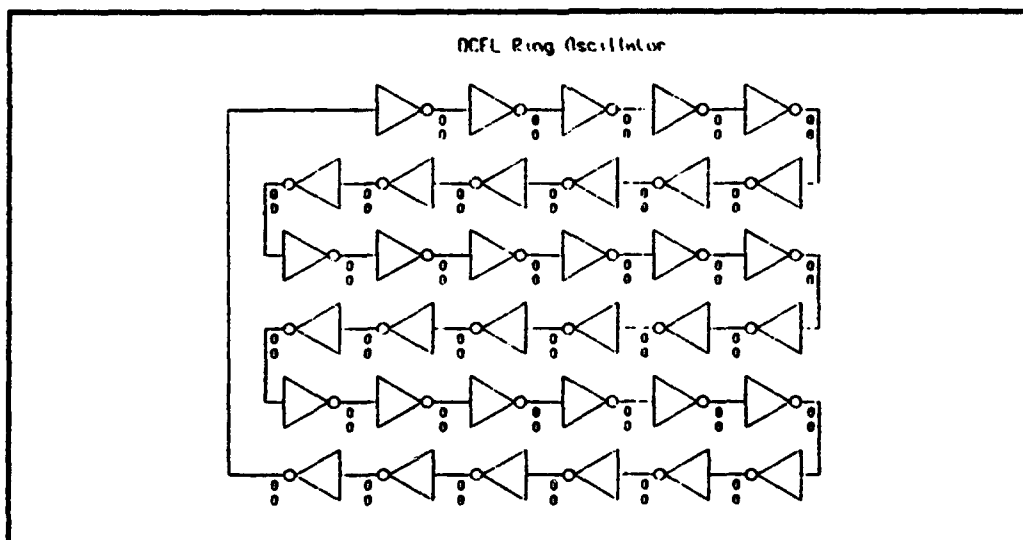


Figure 32 DCFL Ring Oscillator Schematic

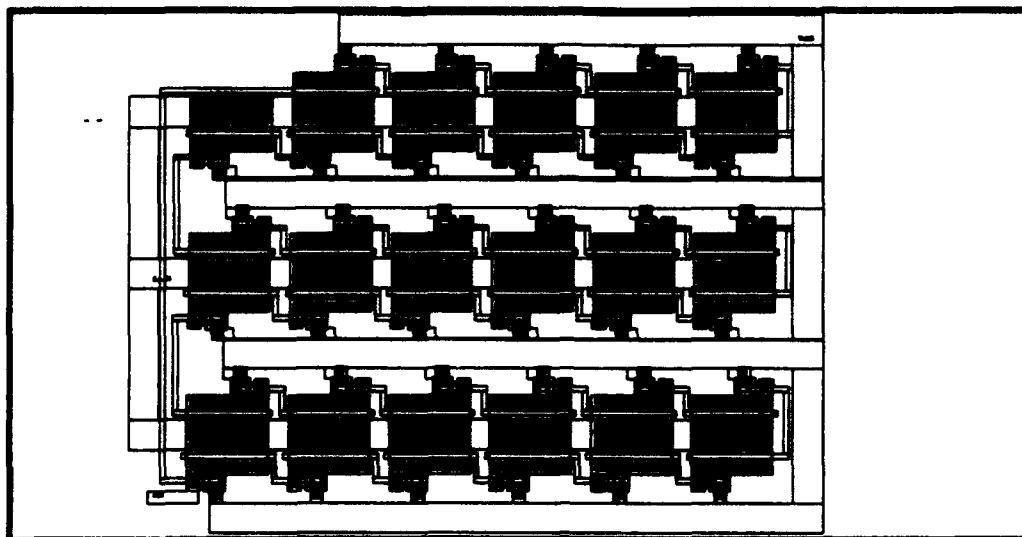


Figure 33 DCFL Ring Oscillator Layout

The four phase clock generation circuit required to drive the FDML circuits was designed using DCFL with a clock signal that shifts between 0.0 volts and 0.6 volts. Since the clock inputs of an FDML circuit are depletion mode FETS, they require a clock signal with a low value of -1.2 volts to turn them "off". Voltage level shifting logic (Figure 34) was added to the output of the clock generation circuit in order to achieve the proper clock values. The resulting circuit layout is shown in Figure 36.

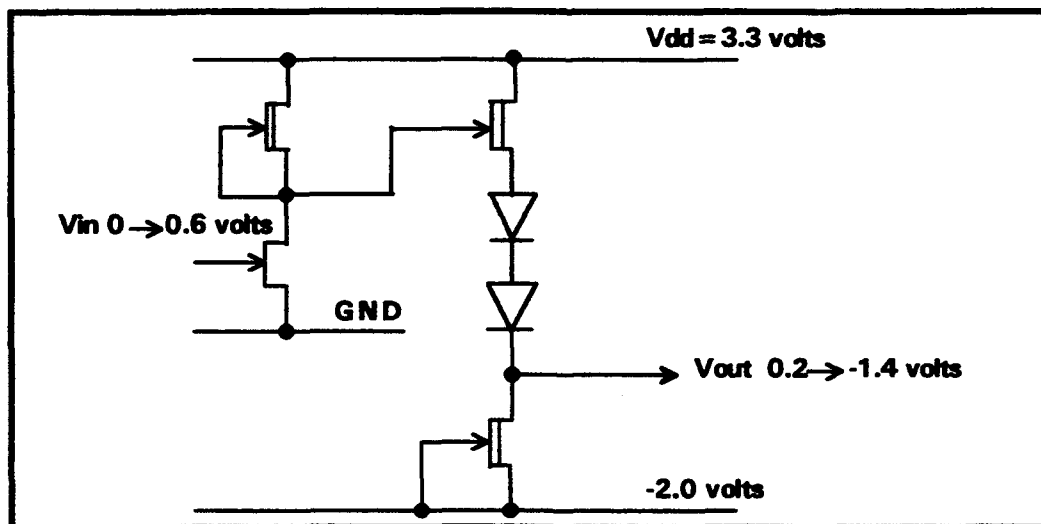


Figure 34 Clock Voltage Shifter Layout

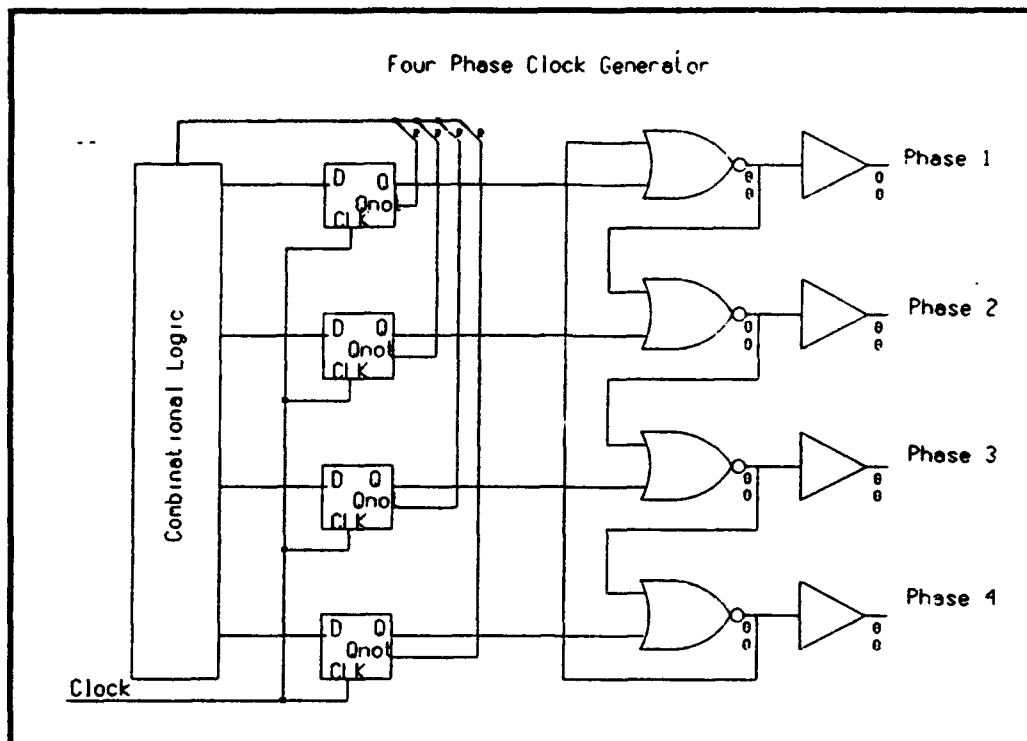


Figure 35 DCFL Four Phase Clock Generation Circuit Schematic

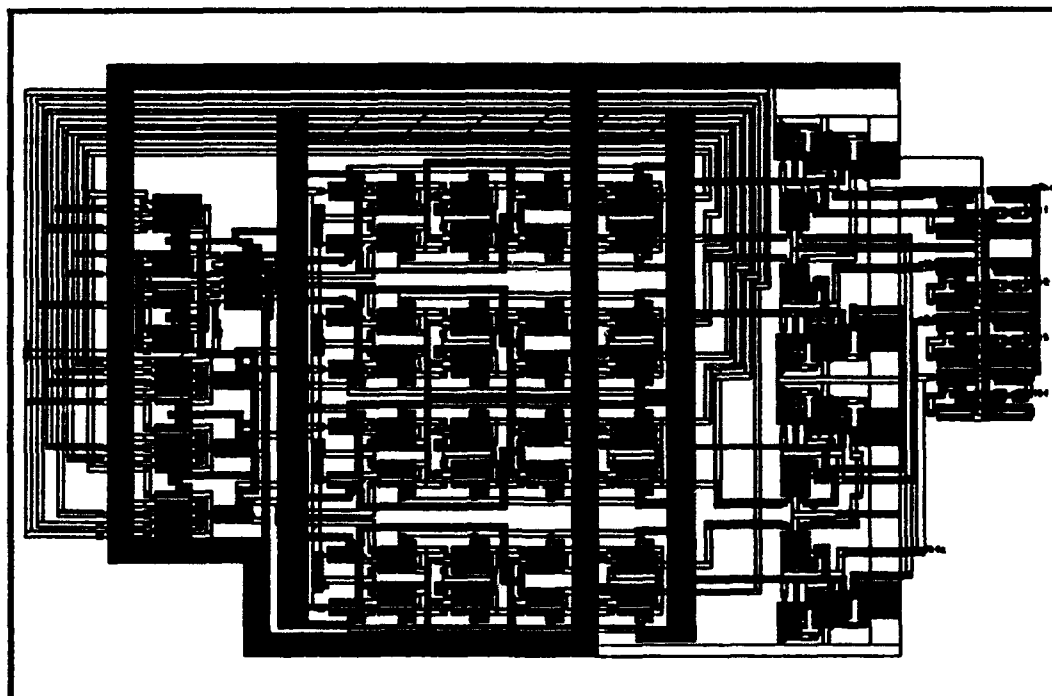


Figure 36 DCFL Four Phase Clock Generation Circuit Layout

## C. FDML CIRCUITS

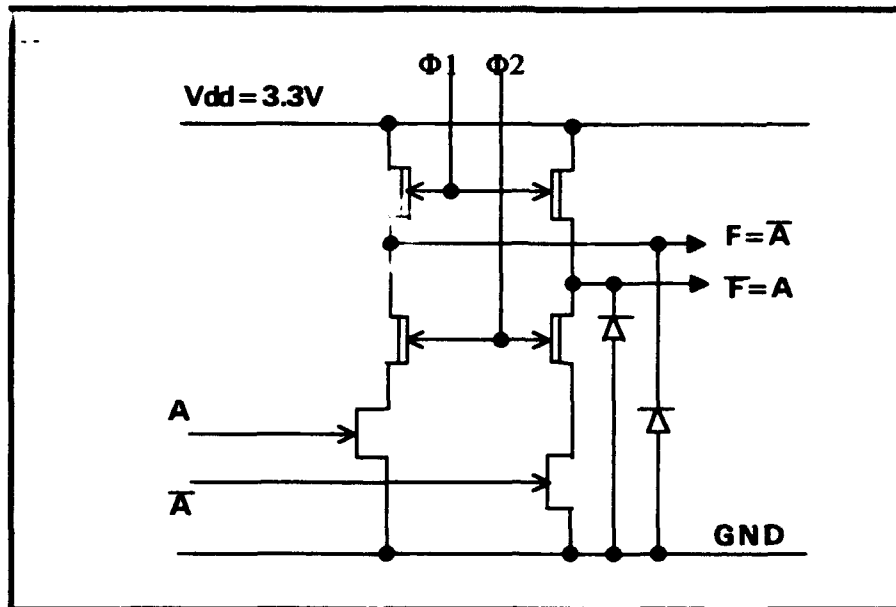


Figure 37 FDML Inverter Schematic

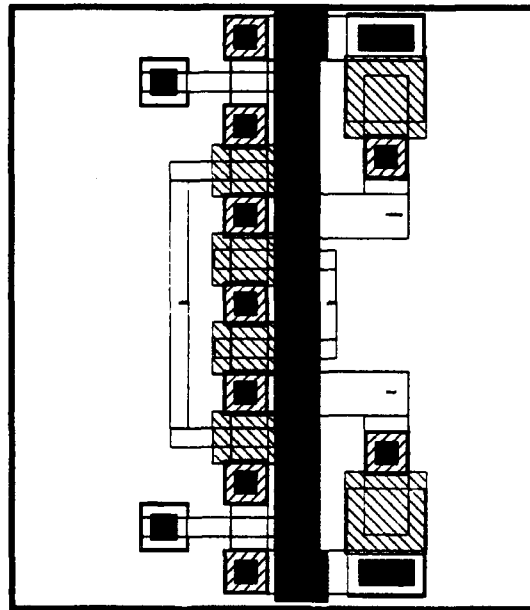


Figure 38 FDML Inverter Layout



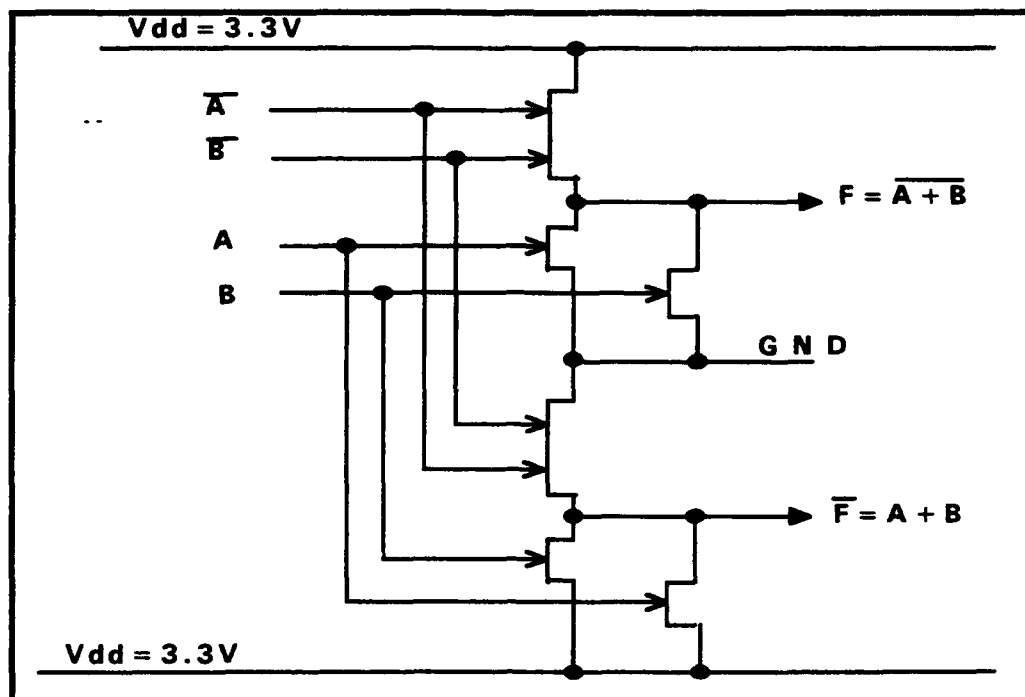


Figure 39 FDML NOR Gate Schematic

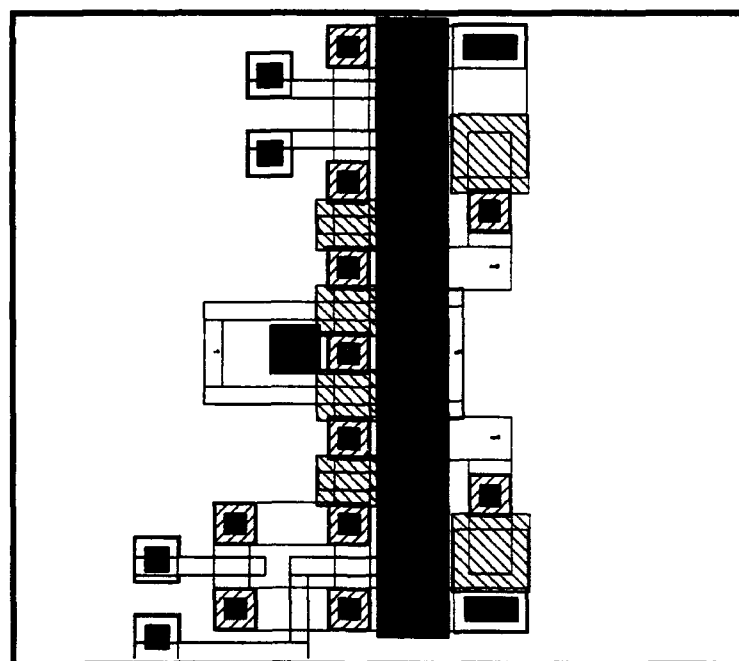


Figure 40 FDML NOR Gate Layout

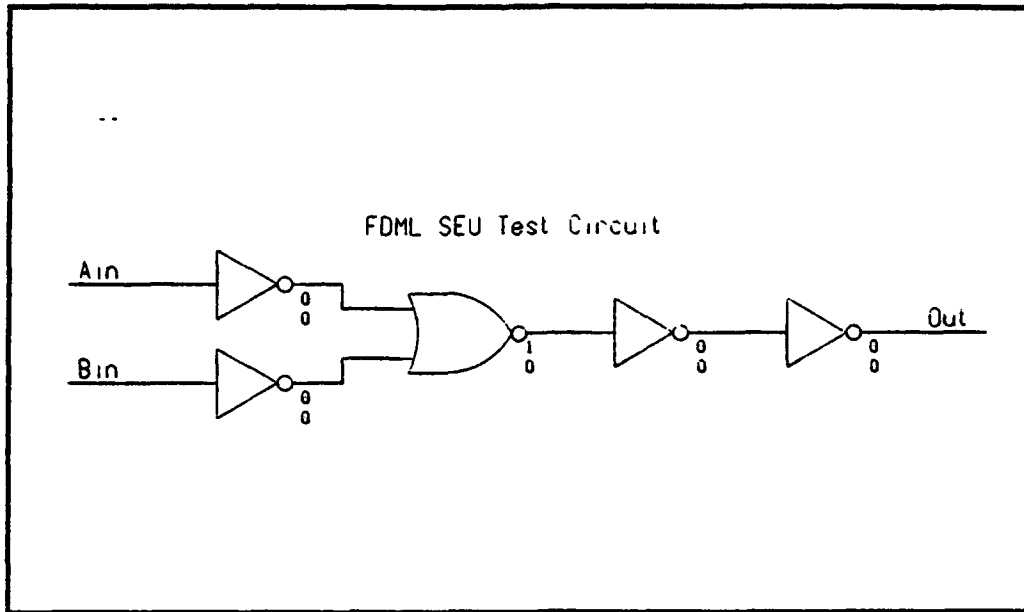


Figure 41 FDML SEU Test Circuit Schematic

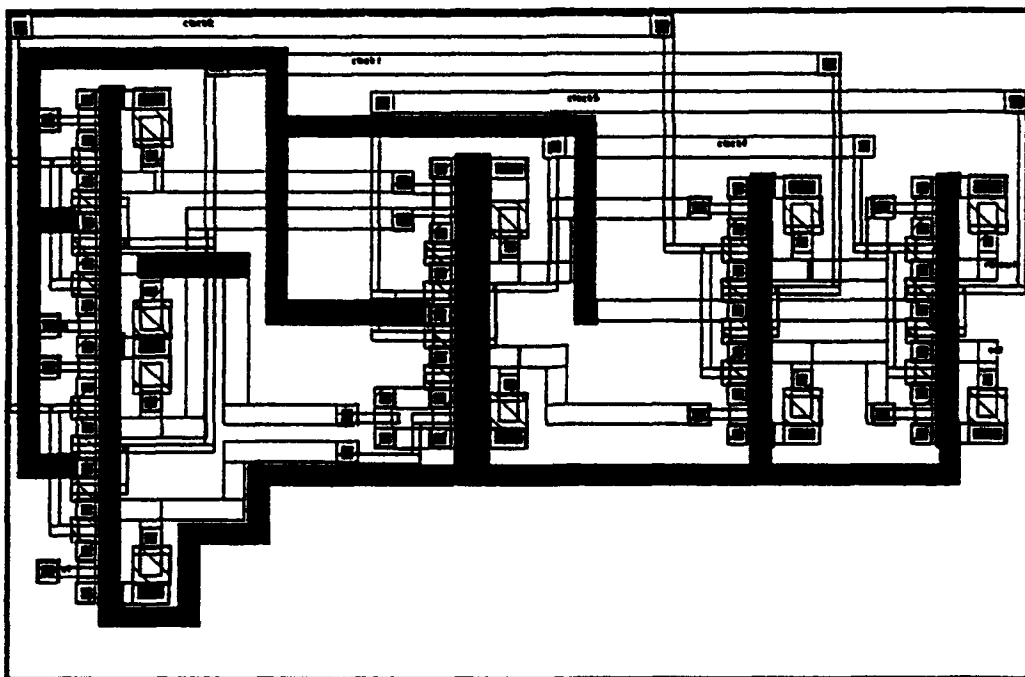


Figure 42 FDML SEU Test Circuit Layout

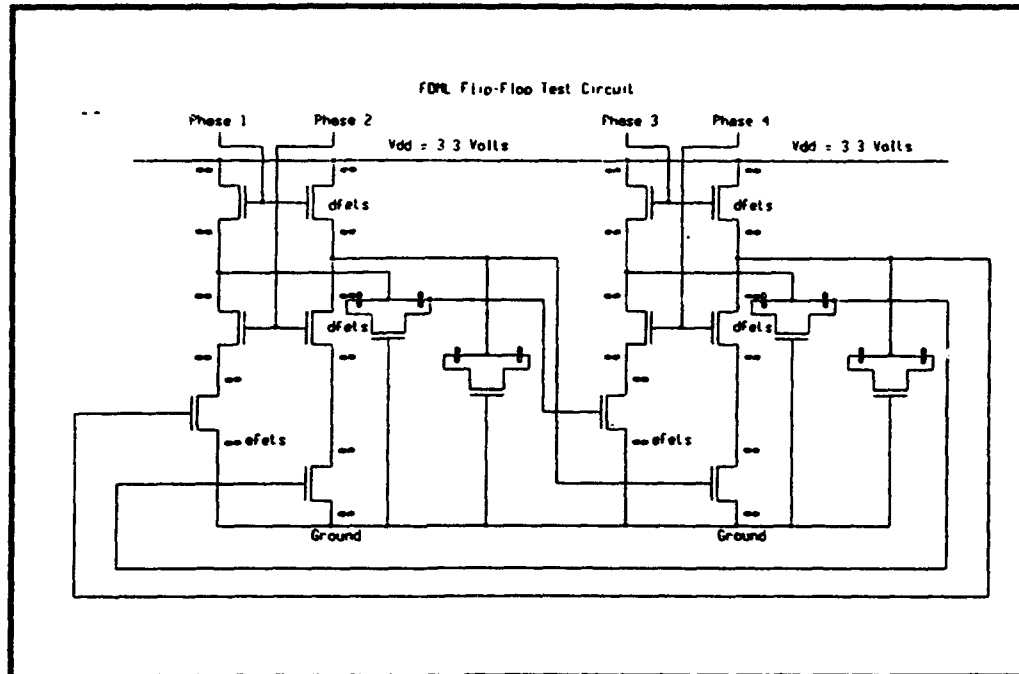


Figure 43 FDML Flip-Flop Schematic

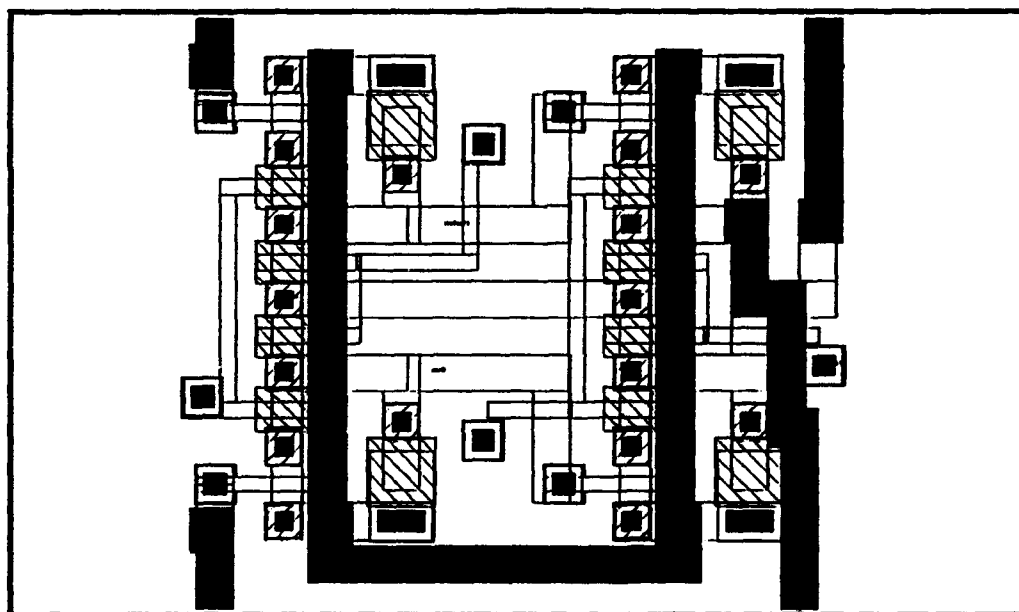


Figure 44 FDML Flip-Flop Layout

## D. COMPLETED CHIP

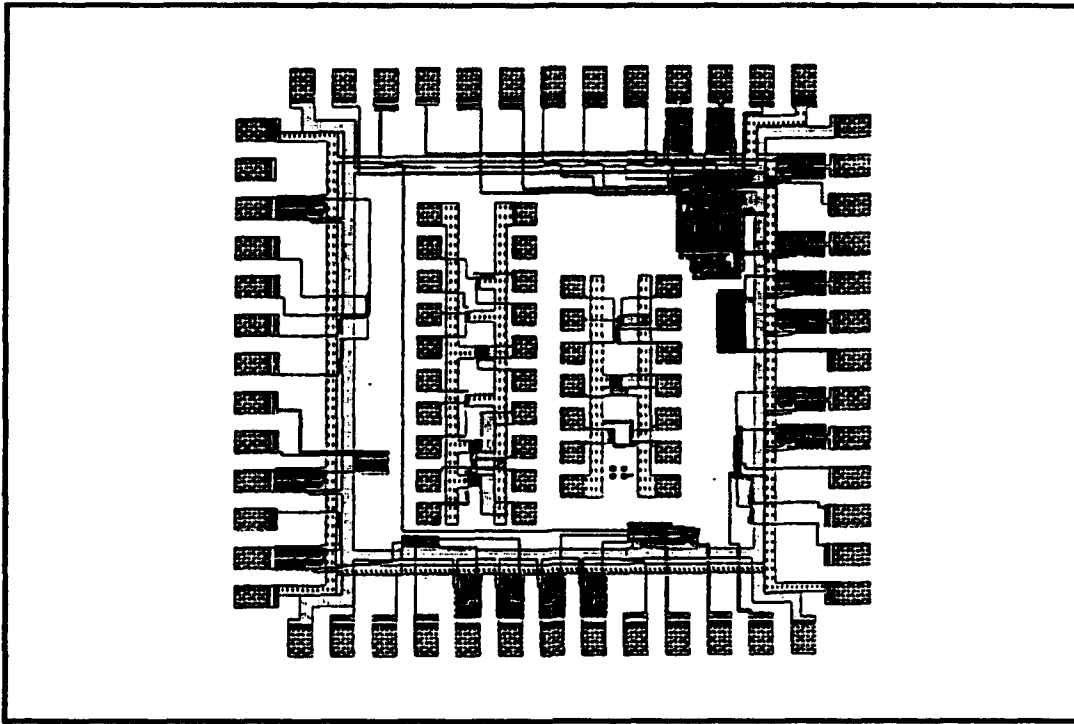


Figure 45 Completed Chip Layout

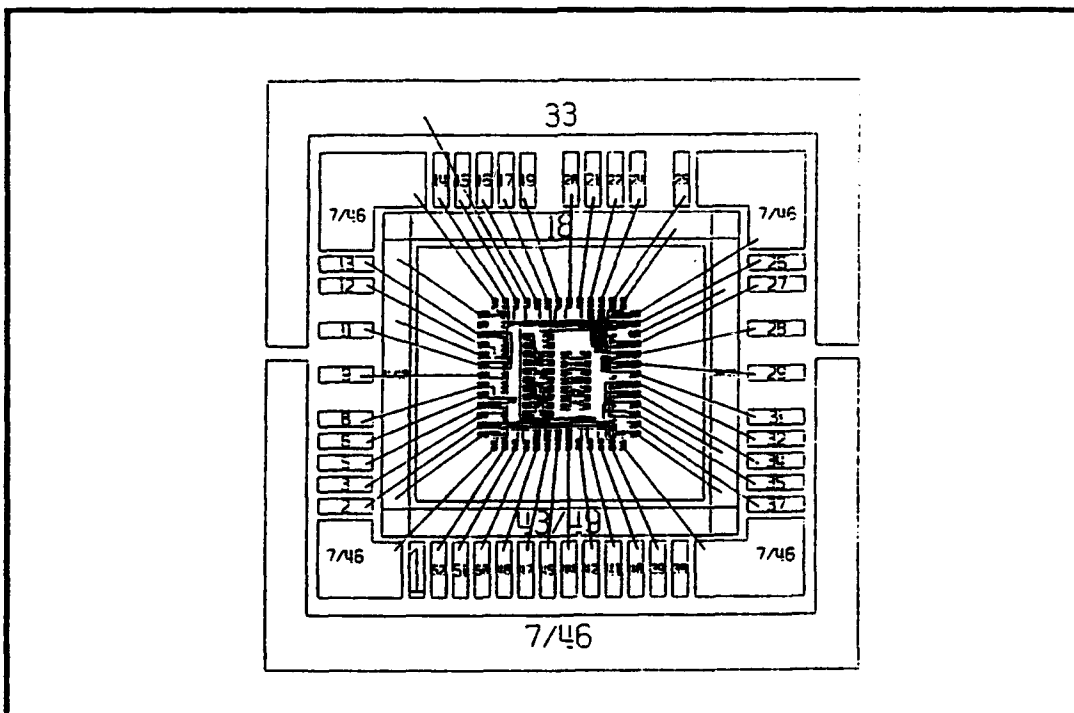


Figure 46 Bonding Diagram for Chip

## **V. COMMENTS AND CONCLUSIONS**

### **A. SEU SIMULATION USING HSPICE**

The first part of this thesis presented the results of extensive computer simulations of single event upsets in a gallium arsenide two phase dynamic MESFET logic circuit. In most cases, HSPICE simulations of the SEUs yielded results that were within an order of magnitude of those obtained by the laser testing technique.

It was found that the exact point of impact of an ion within the integrated circuit is as critical as the amount of charge it deposits. A disadvantage of using HSPICE to simulate SEUs is the inability to model a pulsed, exponential current source at a pinpoint location. It was therefore determined that HSPICE simulation of GaAs circuits is not sufficient to characterize their behavior when exposed to ionizing radiation. It could, however, be used as an estimate of circuit performance prior to fabrication.

### **B. NEW GAAS CIRCUITS**

The second part of this thesis concentrated on the development of GaAs I.C. topologies which would be less susceptible to SEUs. Two new topologies were introduced, pseudo complimentary MESFET logic (PCML) and four phase dynamic MESFET logic.

Of the two new topologies developed, PCML appears to be the most promising. The two most distinguishing factors of PCML gates over other families of logic are its anticipated low static power consumption and a low sensitivity to single event upsets.

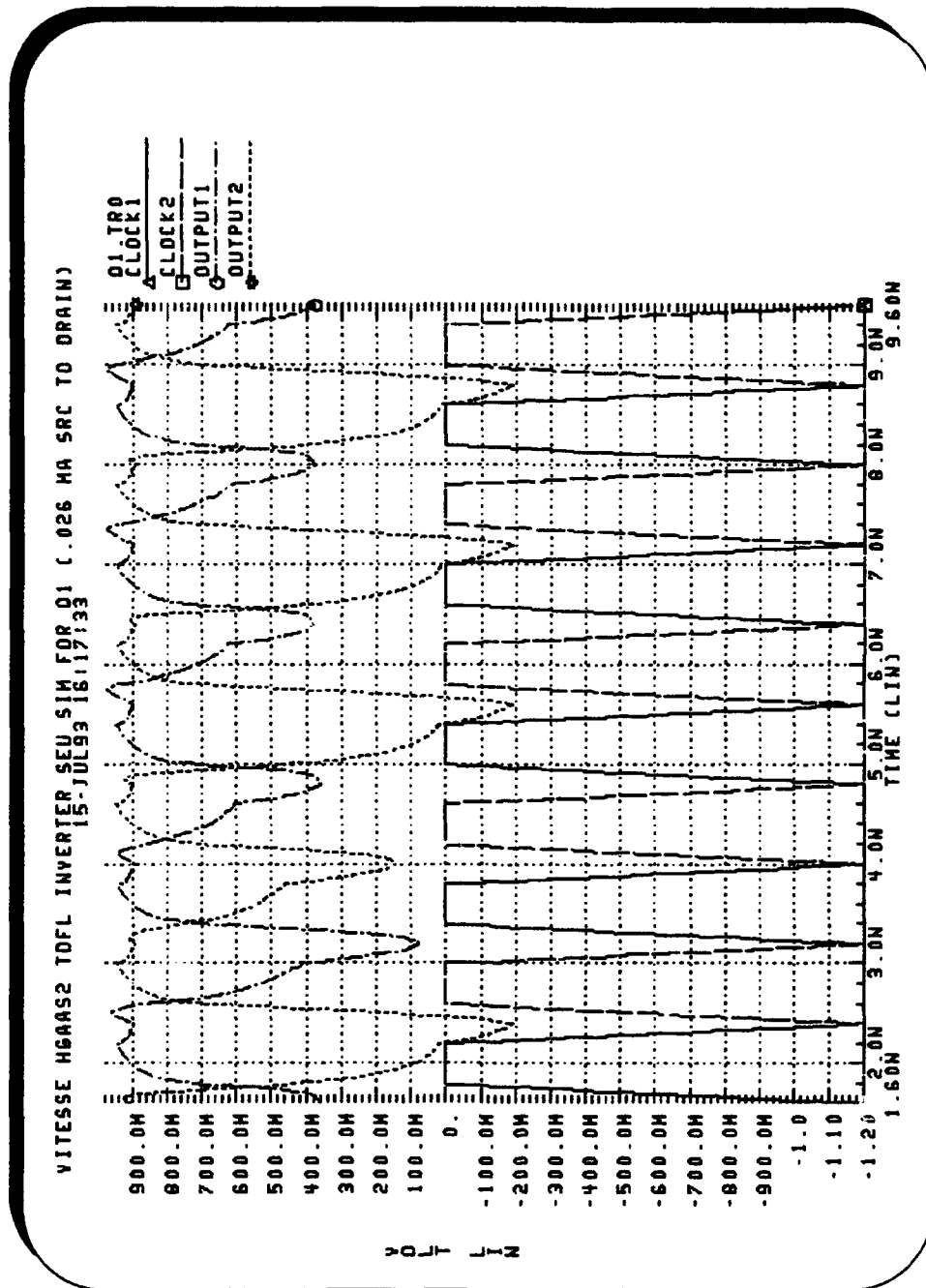
Although the pseudo-complimentary MESFET logic topology is compatible with the low voltage I.C. standard (3.3 volts), it is apparent that it will operate satisfactorily even when utilizing a much lower voltage rail.

The use of a lower voltage rail will decrease the amount of current conducted through the Schottky barrier diodes which are present at the inputs of each logic gate. The anticipated reduction in power dissipation obtained at lower operating voltages could lead to an increased number of logic gates per chip due to decreased operating temperatures. Also, reducing the power rail voltages would not significantly reduce the operating frequency of the circuits.

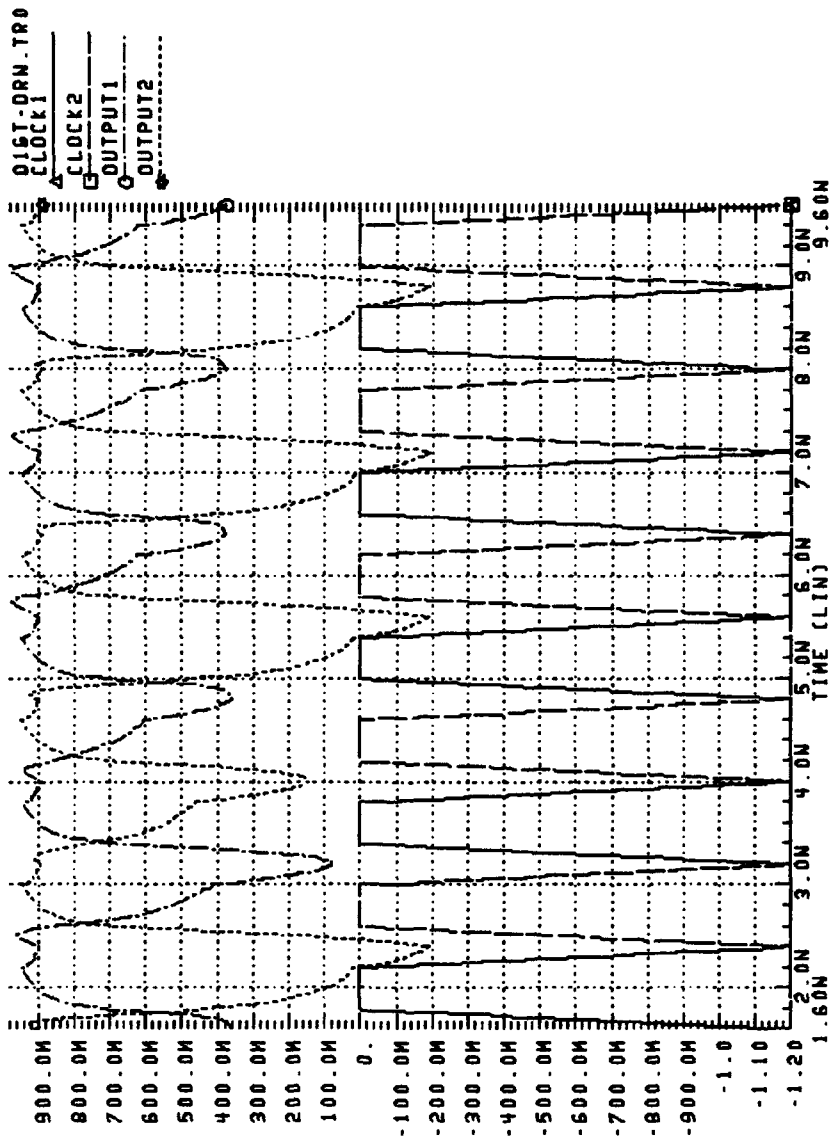
## **C. RECOMMENDATIONS FOR FUTURE RESEARCH**

Future research should include the test and evaluation of the experimental I.C. developed for this thesis. If the operation of the various topologies introduced show a significant improvement in SEU tolerance coupled with a low power budget, as predicted, the implementation of a practical integrated circuit which uses them should be considered.

# APPENDIX A - SEU SIMULATIONS

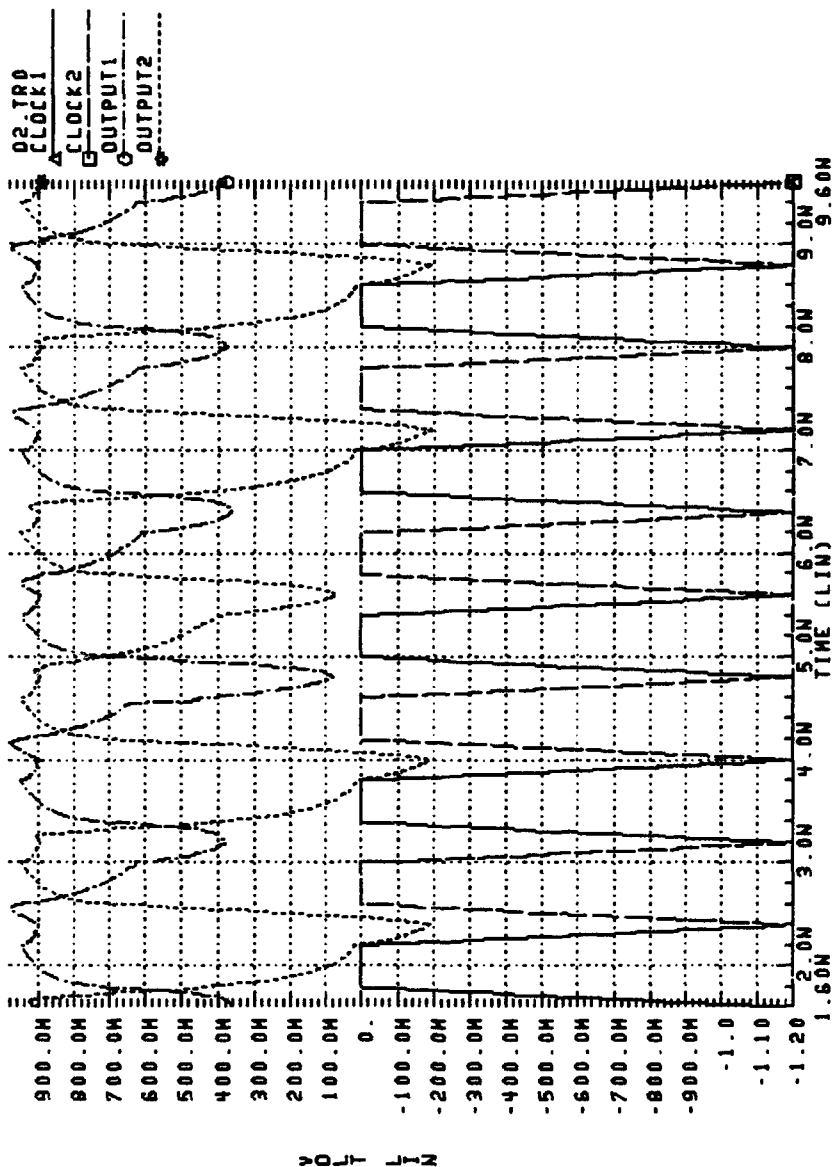


VITESSE H6AAS2 TOFL INVERTER SEU SIM FOR Q1 (.026 MA GATE TO DRAIN)  
15 JUL 93 16:24:20

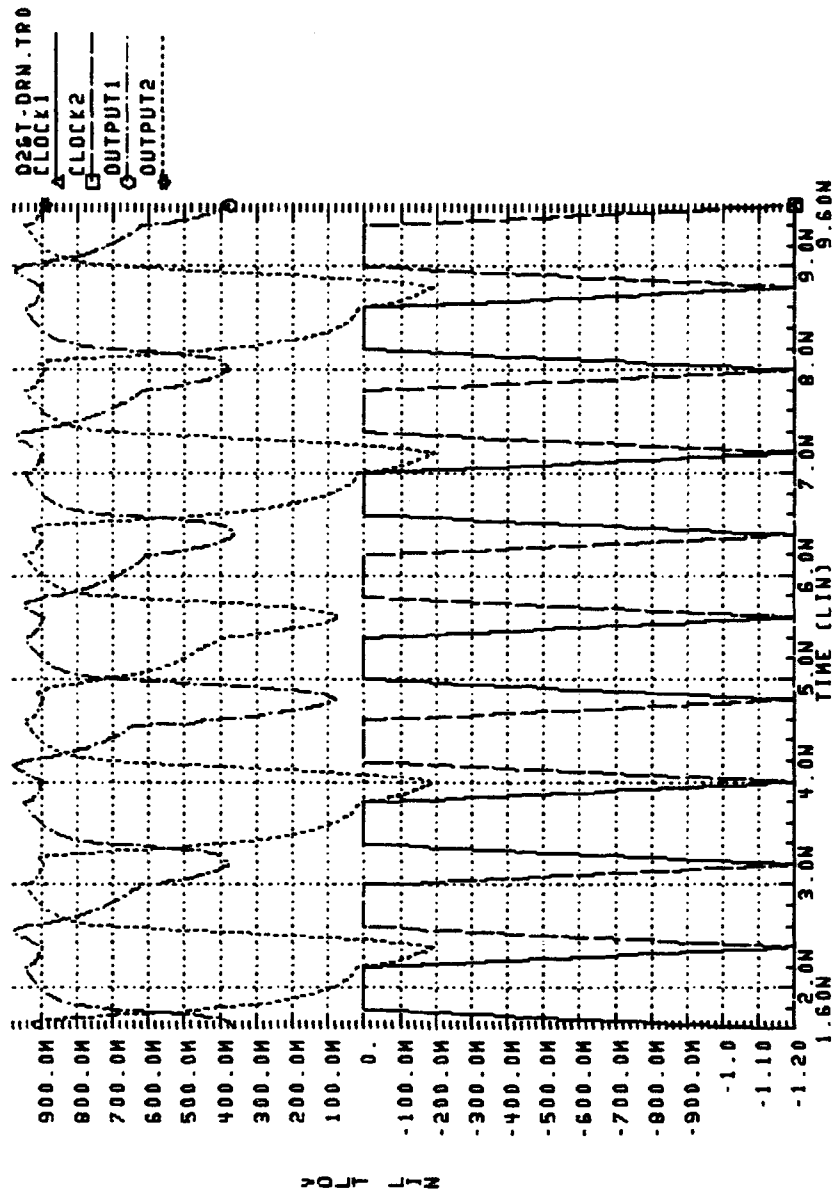




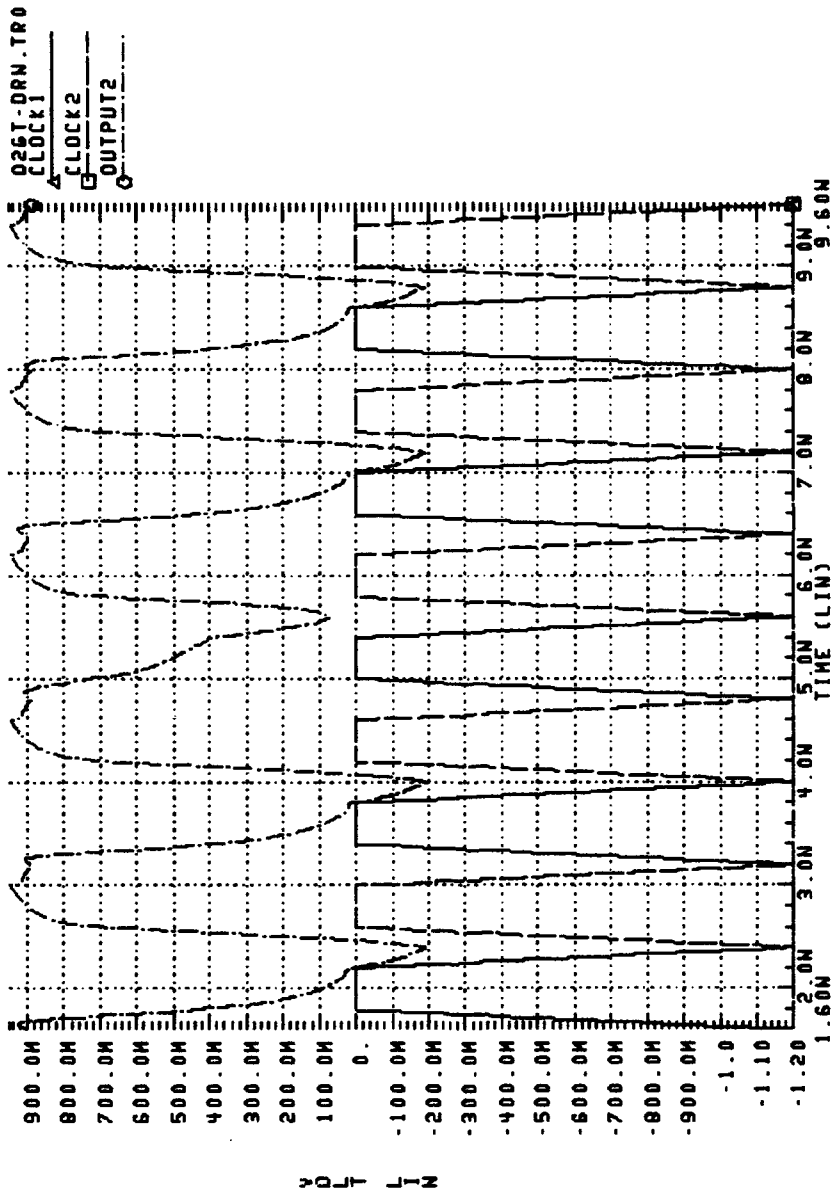
VITESSE HGAAS2 TOFL INVERTER SEU SIM FOR Q2 (.15 MA SRC TO DRAIN)  
19-JUL93 12:43:18



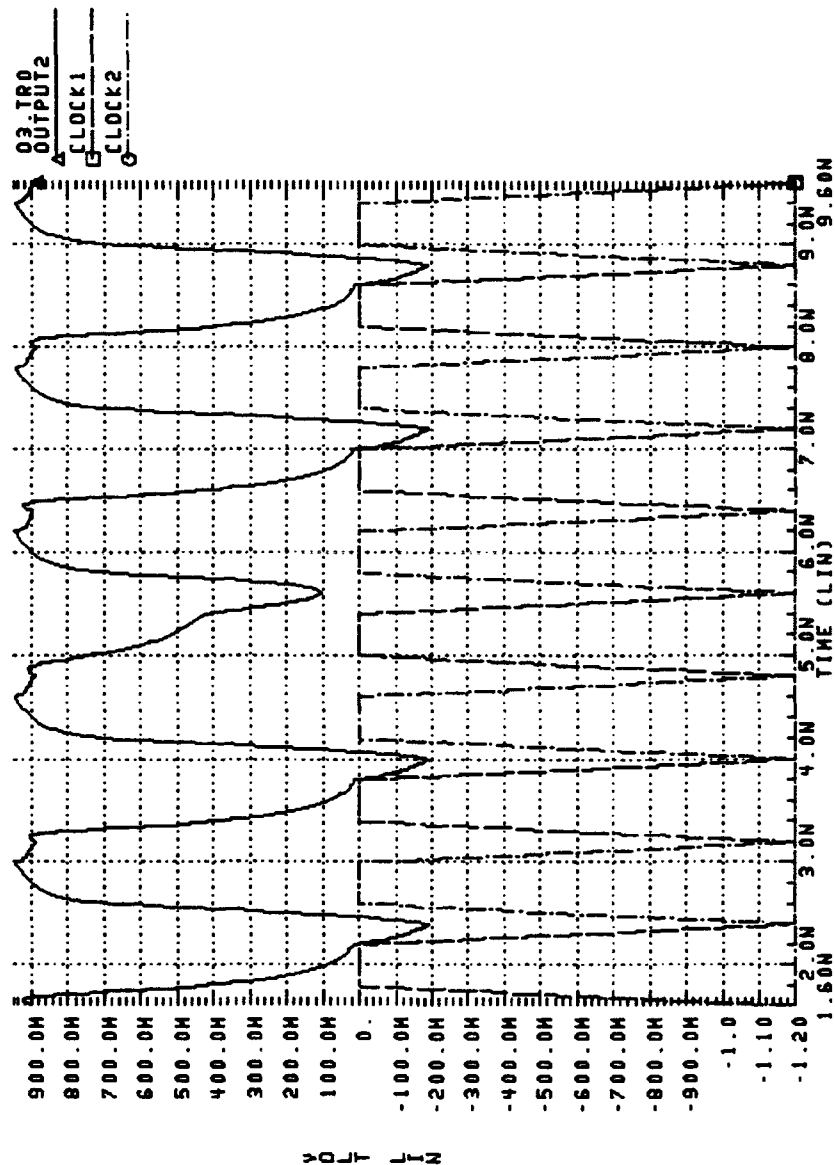
VITESSE H6AAS2 TOFL INVERTER SEU SIM FOR Q2 (.15 MA DRAIN TO GATE)  
 19-JUL93 12:48:41



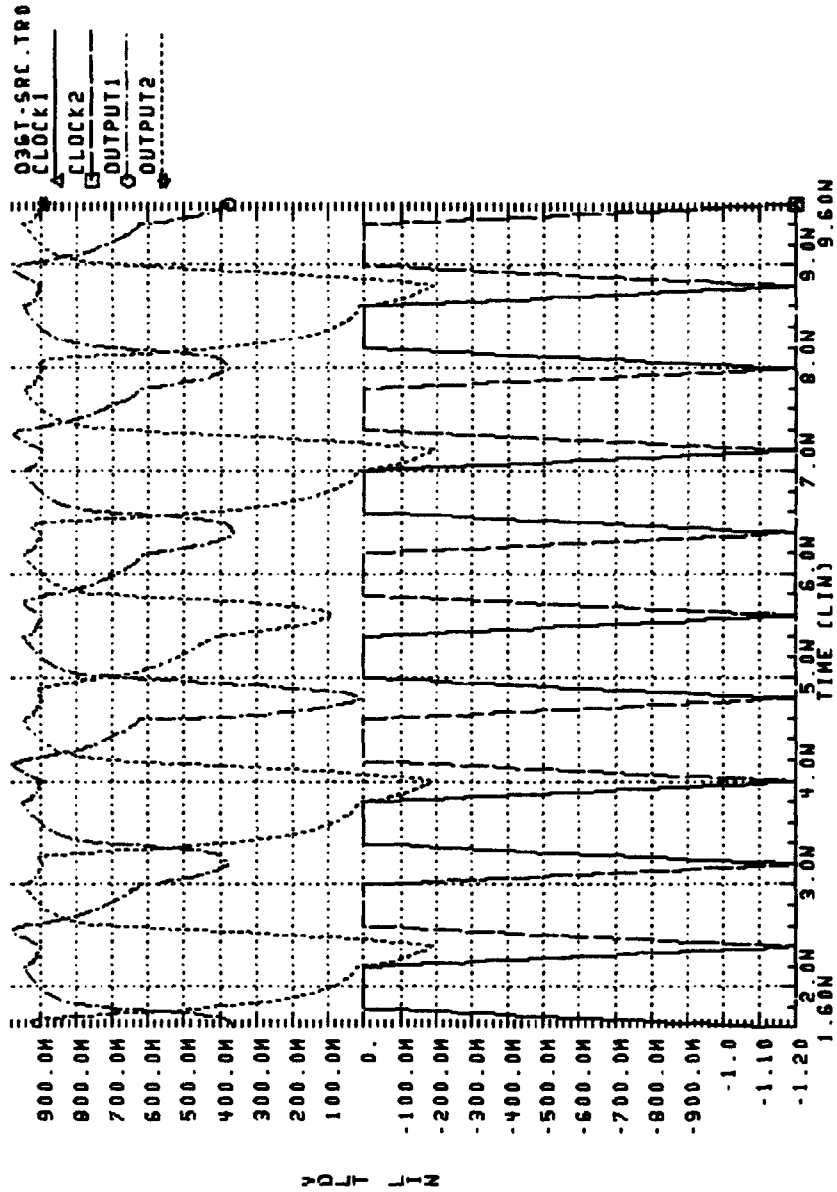
VITESSE H8A952 TDFL INVERTER SEU SIM FOR 02 (.15 MA DRAIN TO GATE)  
19-JUL93 12:48:41



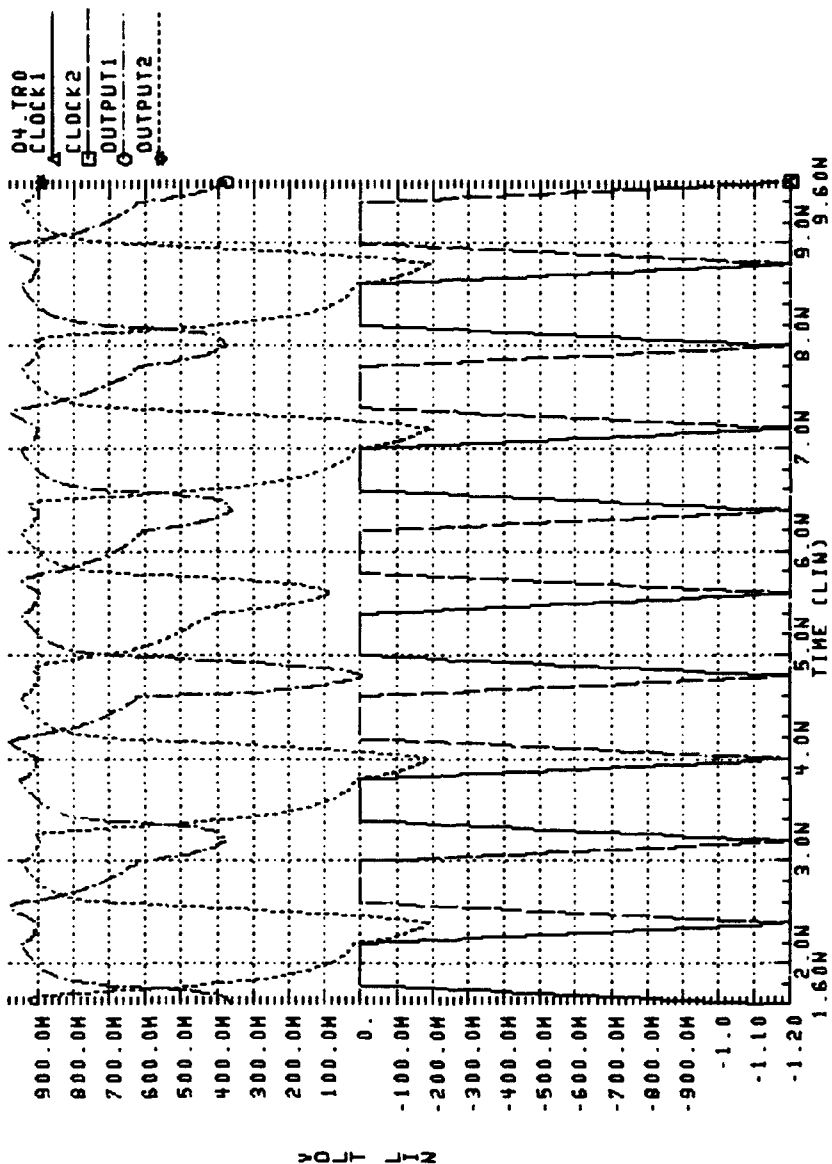
VITESSE H6AAS2 TOFL INVERTER SEU SIM FOR 03 (.65 MA SRC TO DRAIN)  
19-JUL93 12:58:40

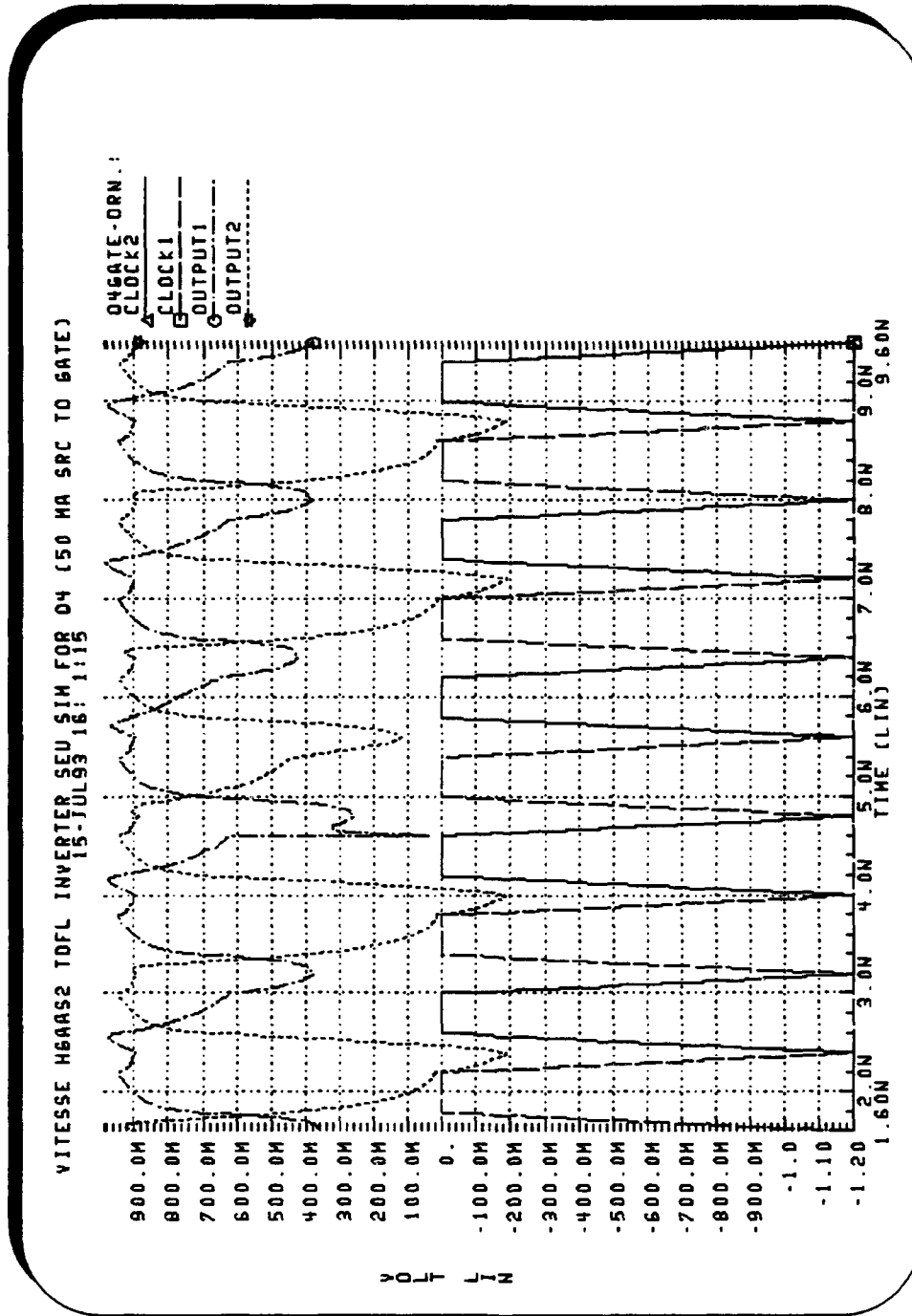


VITESSE HGARS2 TDFL INVERTER SEU SIM FOR Q3 (.175 MA GATE TO SOURCE)  
 14-JUL93 16: 8:52

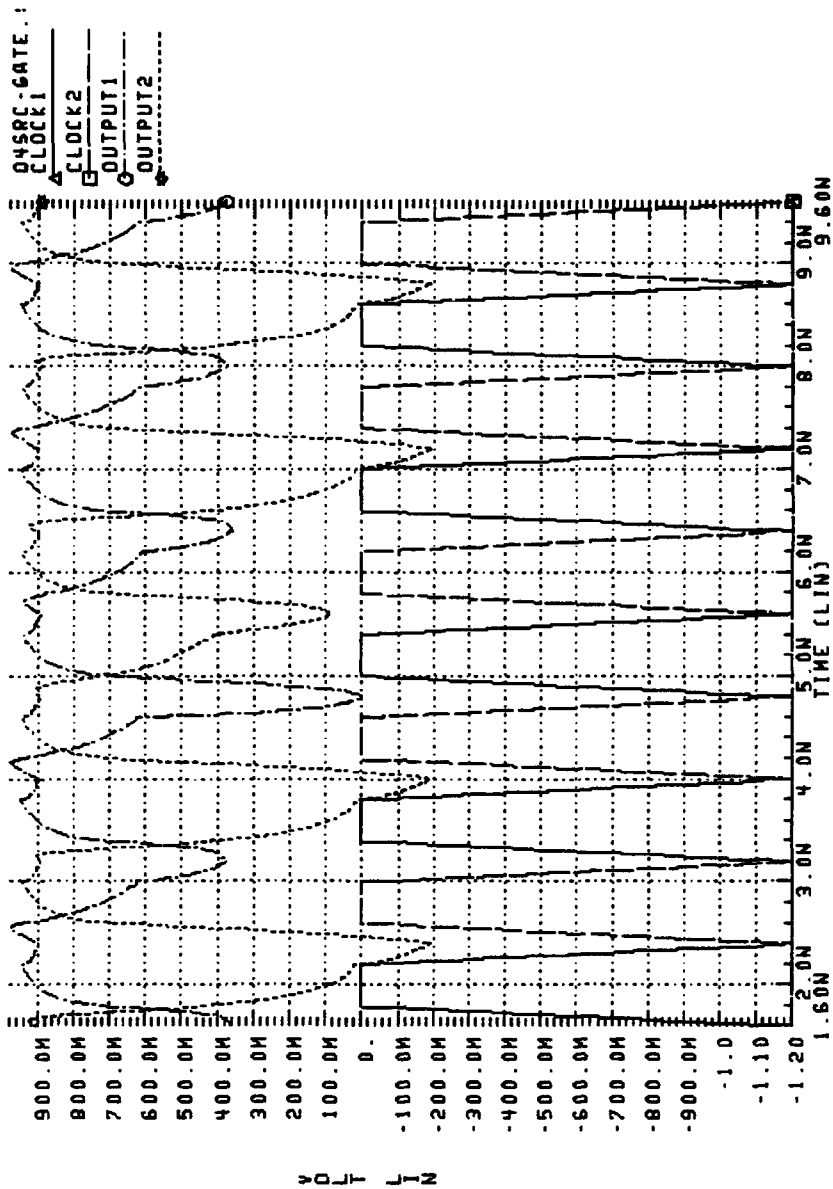


VITESSE H6ARS2 TOFL INVERTER SEU SIM FOR 04 (.10 MA SRC TO DRAIN)  
15-JUL93 15:25:29



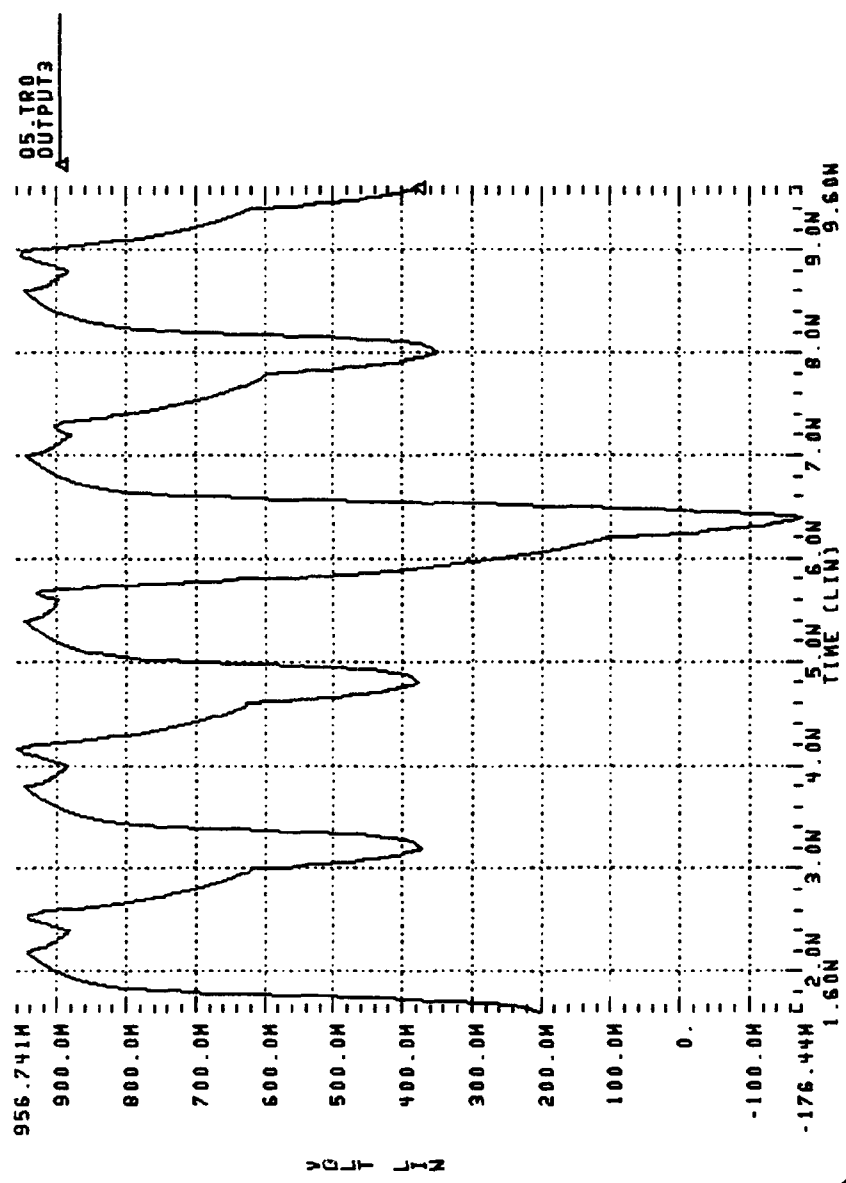


VITESSE HGARS2 TOFL INVERTER SEU SIM FOR 04 (.11 MA SRC TO GATE)  
15-JUL93 15:44:55

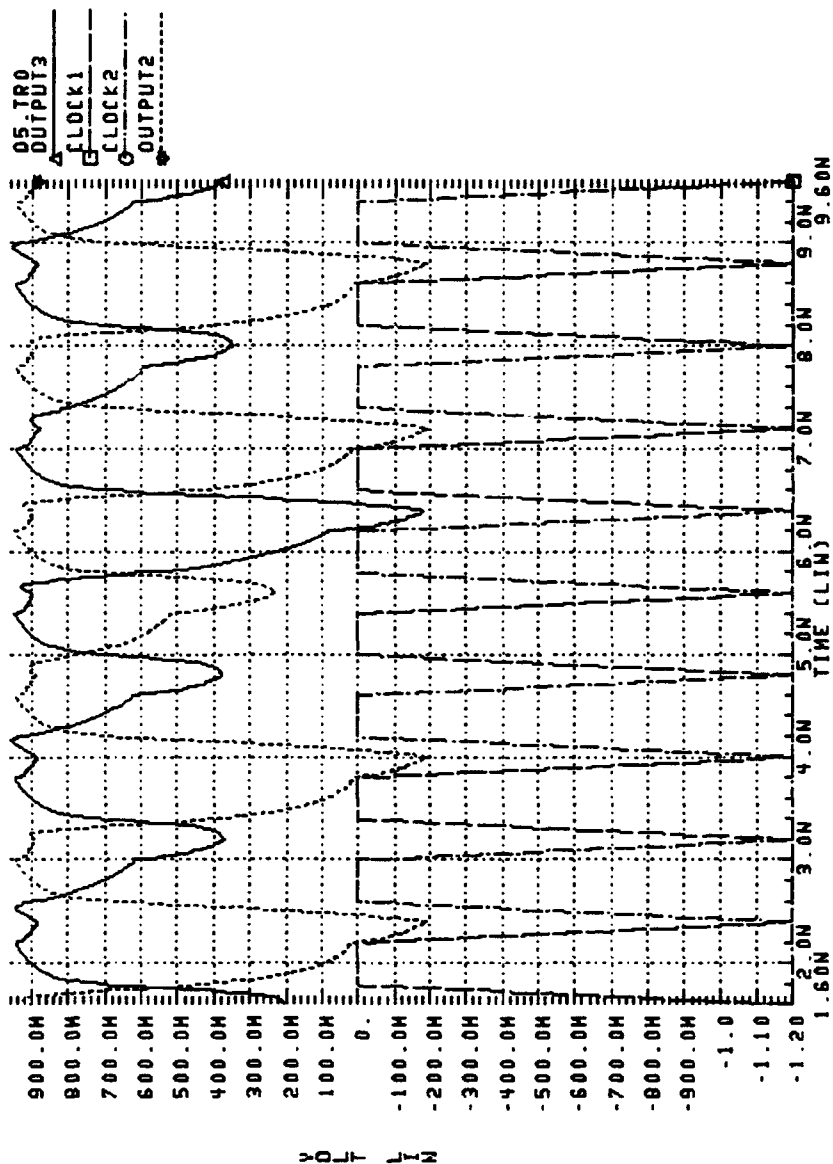




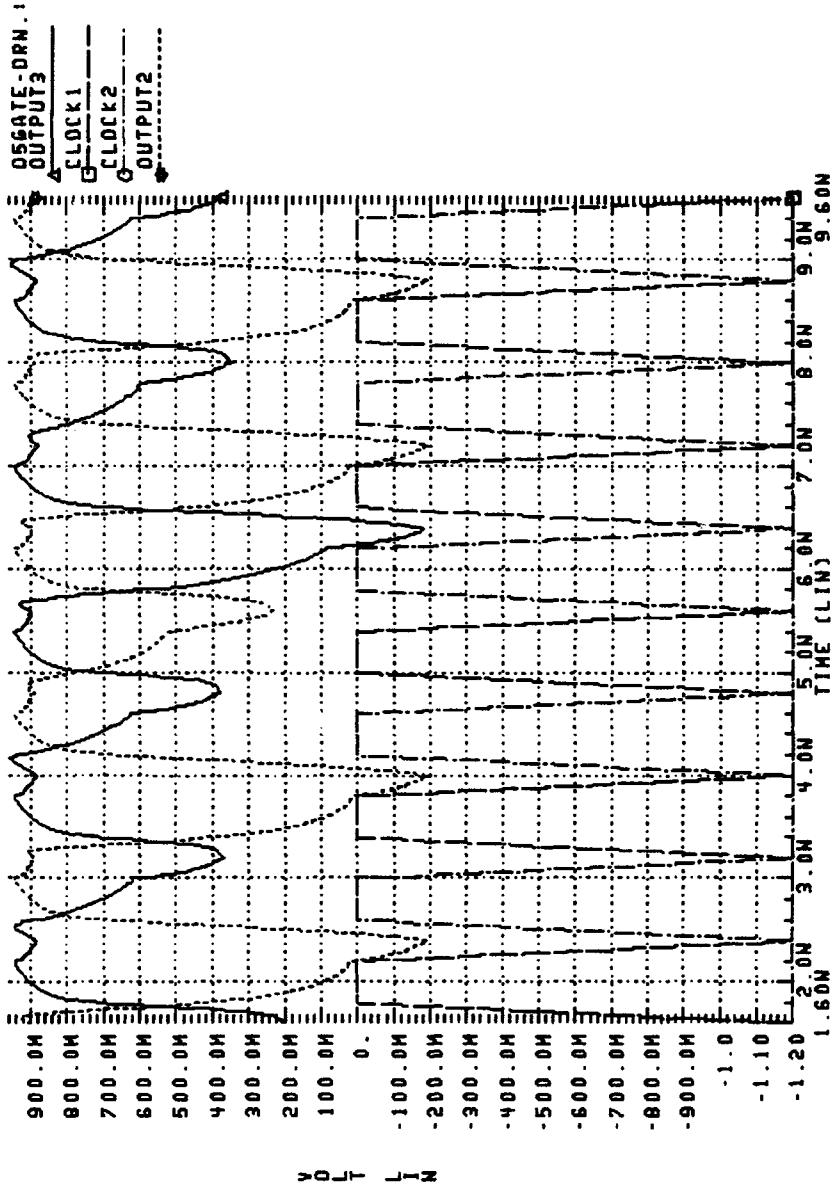
VITESSE H6AAS2 TOFL INVERTER SEU SIM FOR 05 (.18 MA SRC TO DRAIN)  
 21-JUL-93 15:48:58



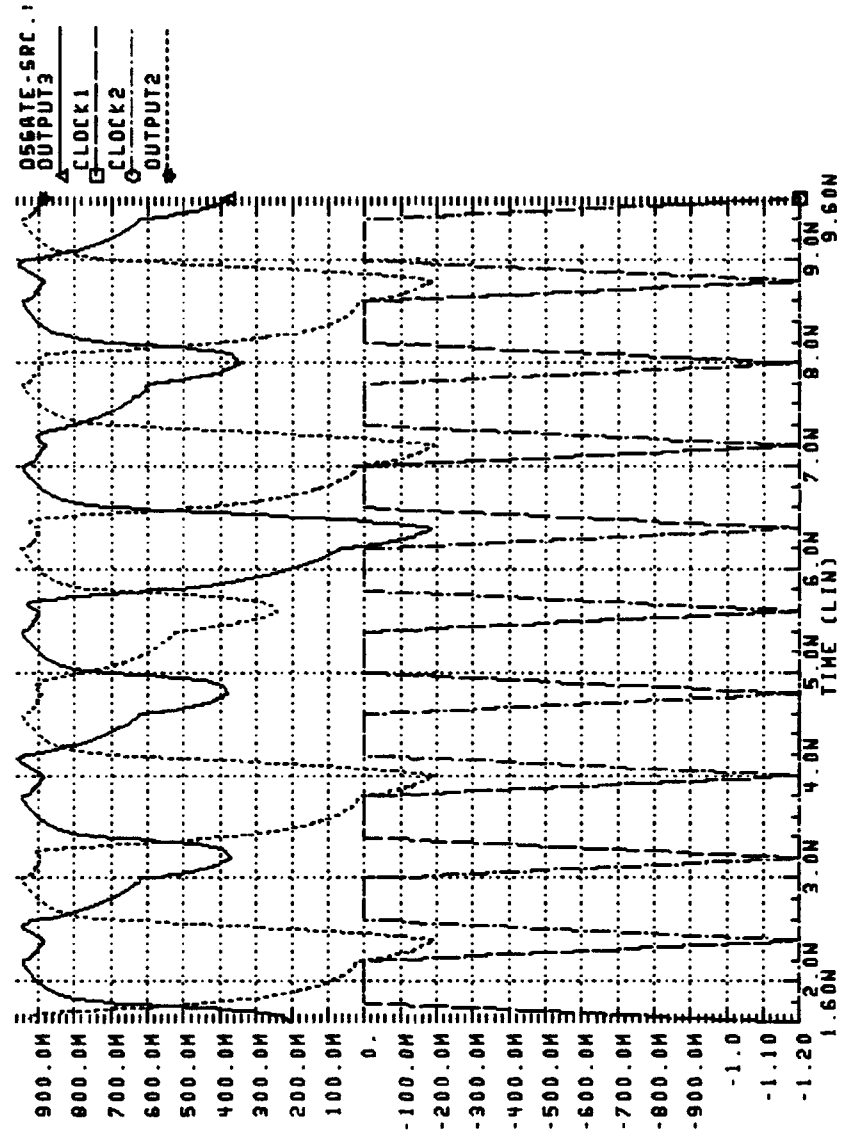
VITESSE HGARS2 TOFL INVERTER SEU SIM FOR 05 (.105 MA SRC TO DRAIN)  
21-JUL93 15:52:15



VITESSE HGAAS2 TDFL INVERTER SEU SIM FOR Q5 (.085 MA GATE TO DRAIN)  
21-JUL93 18:17:38

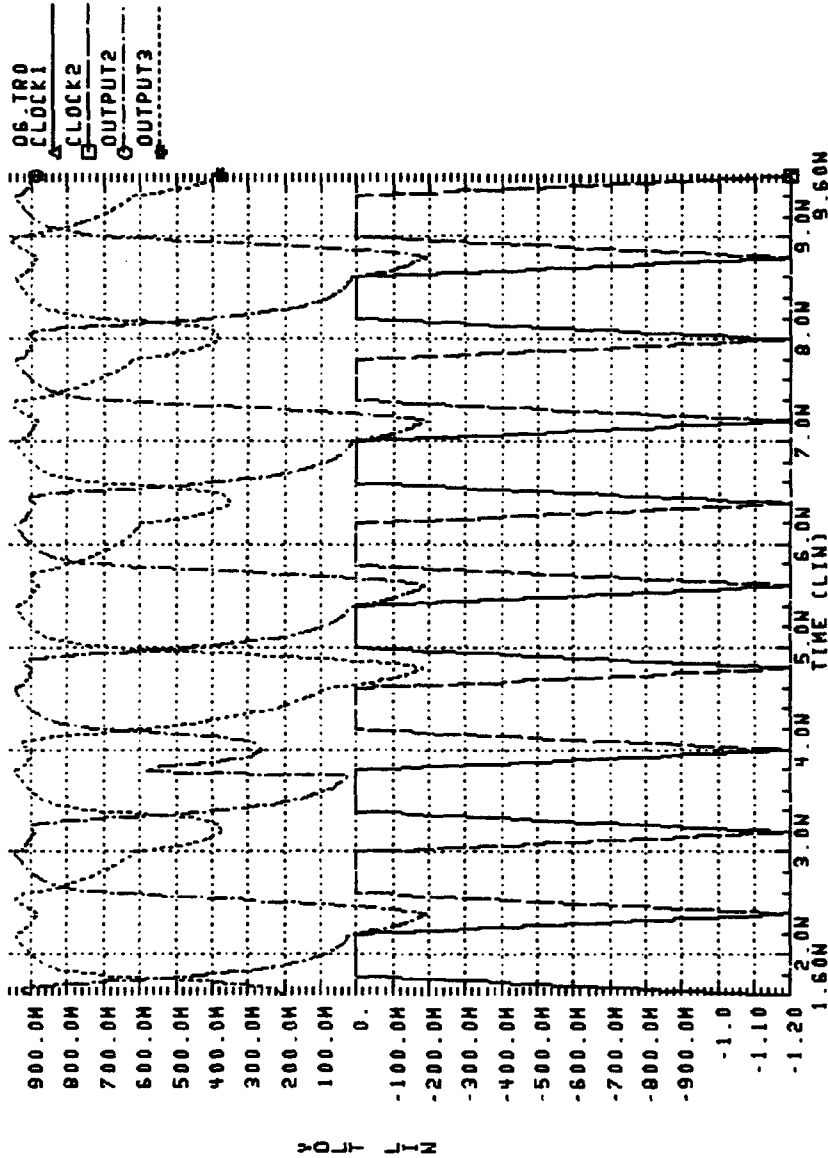


VITESSE H6RA52 TOFL INVERTER SEU SIM FOR 05 (.208 MA GATE TO SOURCE)  
 22 JUL 93 15:38:31

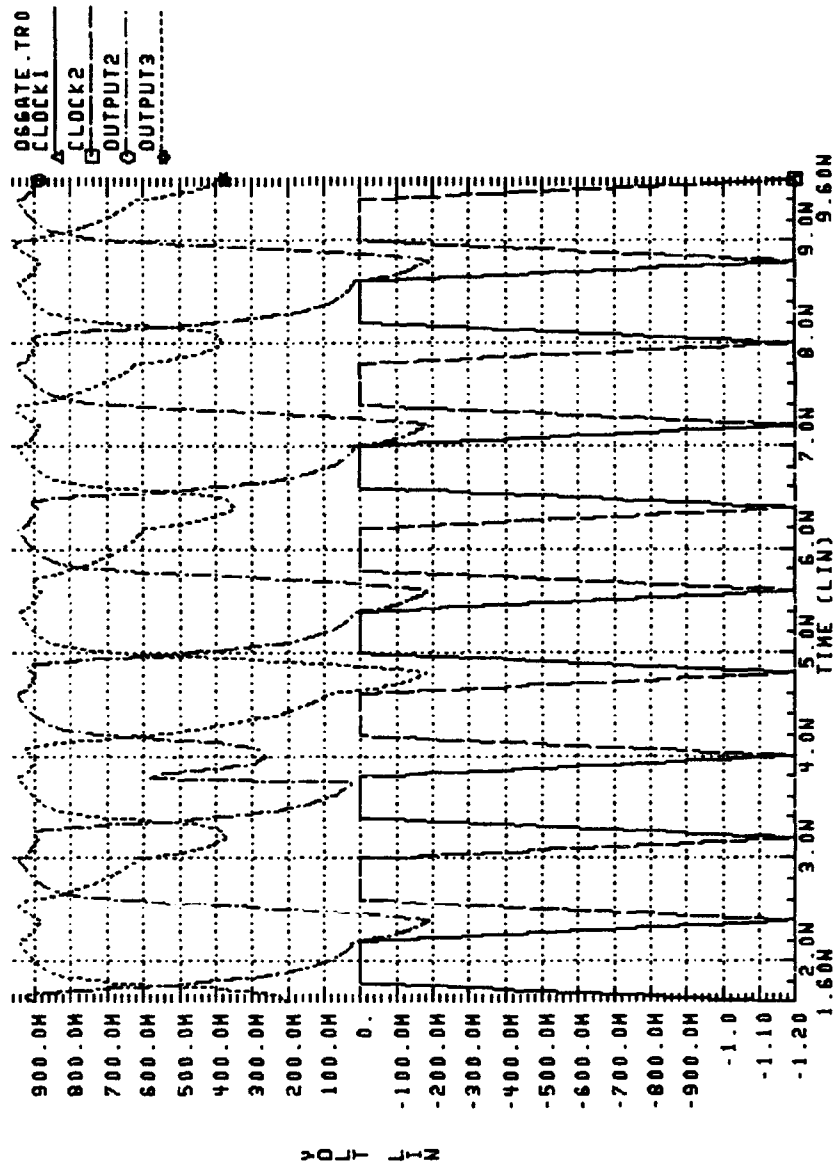


VOLT

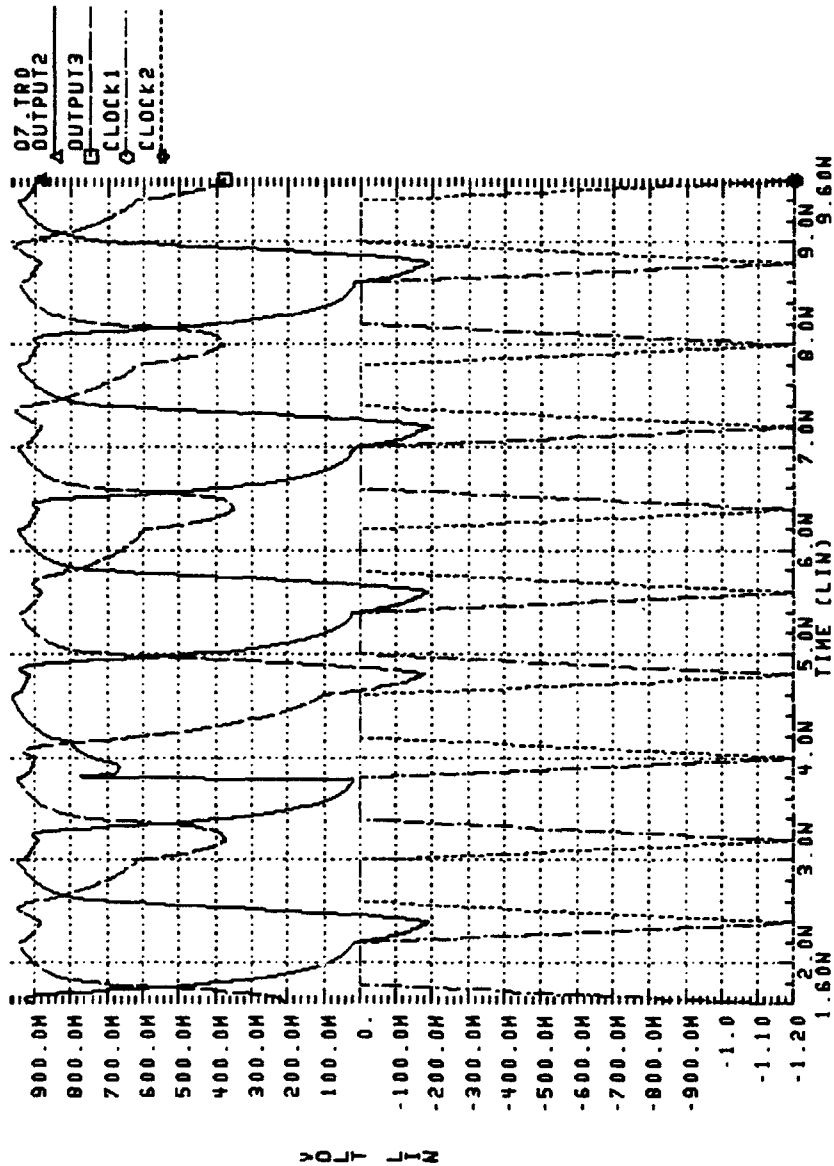
VITESSE H8AAS2 TOFL INVERTER SEU SIM FOR 06 (.55 MA SRC TO DRAIN)  
19-JUL-93 17:41:43



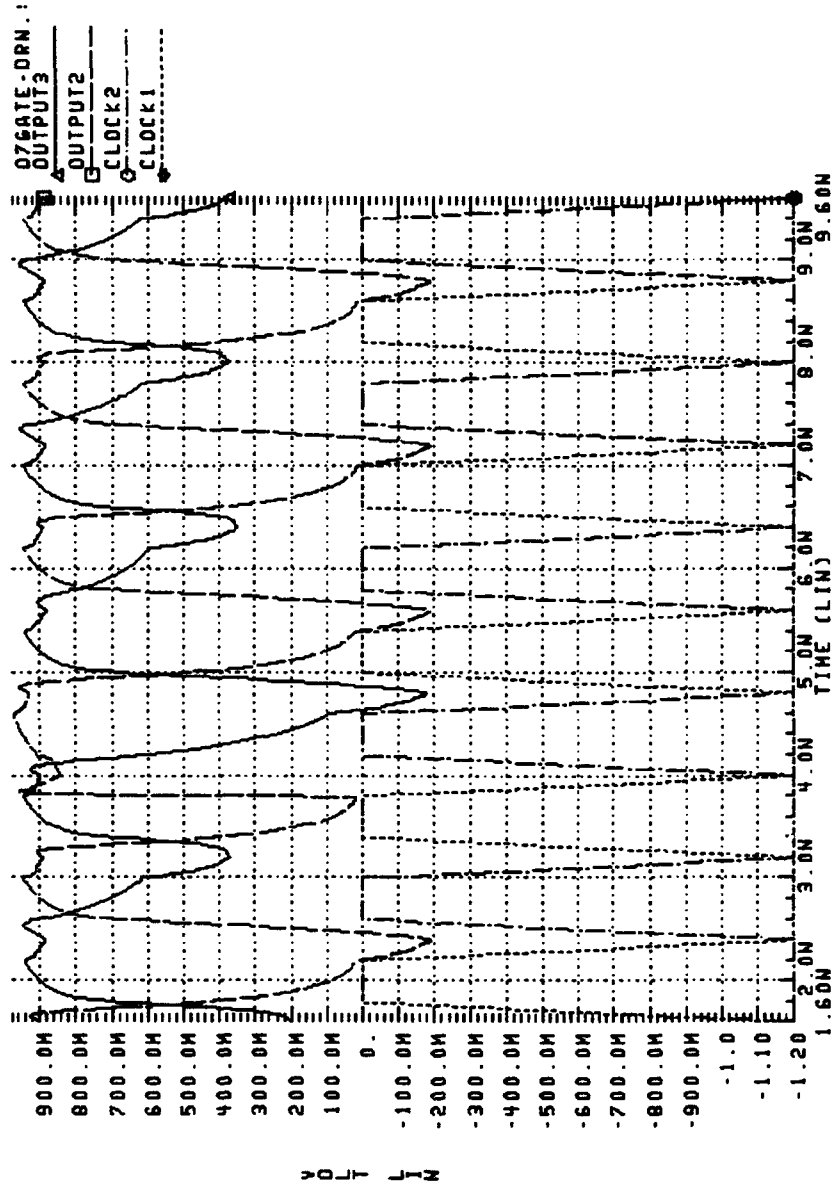
VITESSE H6AAS2 TOFL INVERTER SEU SIM FOR DS (.6 MA GATE TO DRAIN)  
12-JUL93 12:46:44



VITESSE H6AAS2 TDFL INVERTER SEU SIM FOR 07 (2.50 MA SRC TO DRAIN)  
28-JUL93 15:53:31

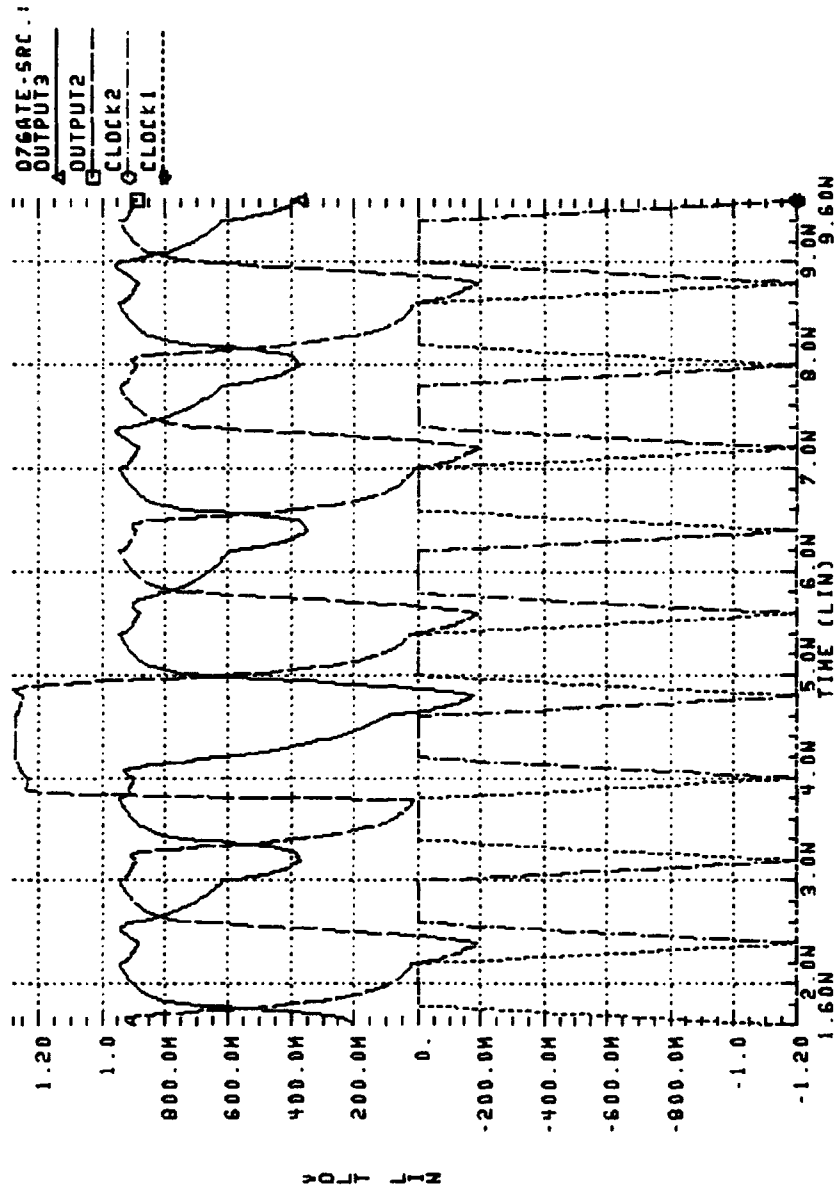


VITESSE HGARS2 TDFL INVERTER SEU SIM FOR 07 (2.50 MA GATE TO DRAIN)  
28-JUL93 16:46:29

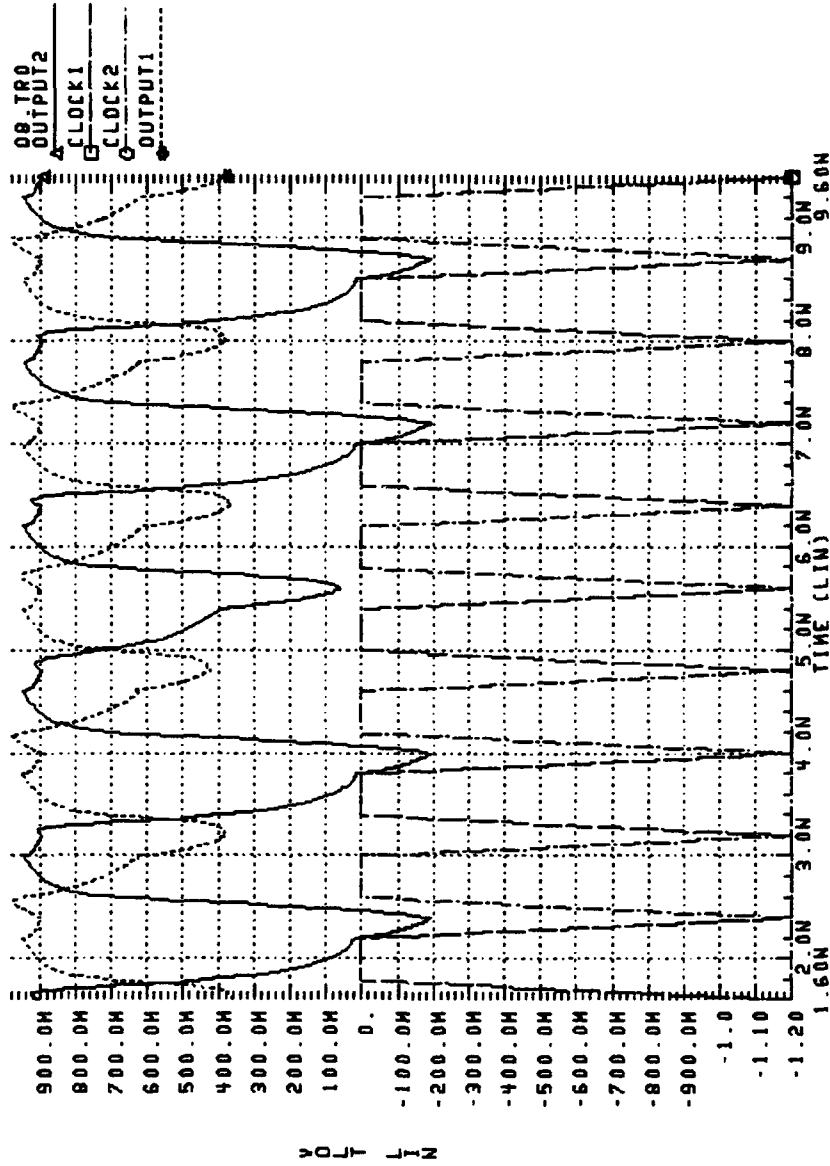




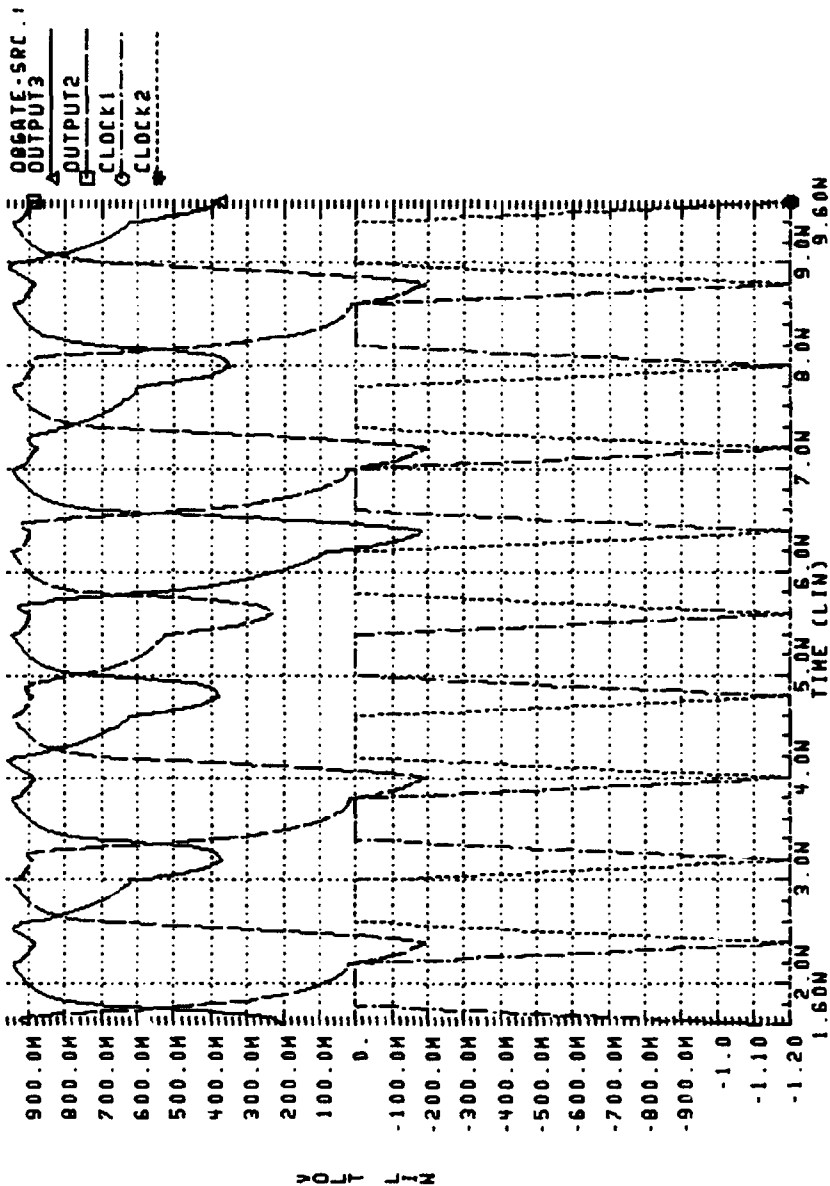
VITESSE HBAR52 TOFL INVERTER SEU SIM FOR 07 (.797 MA SRC TO GATE)  
26-JUL93 17:11:11



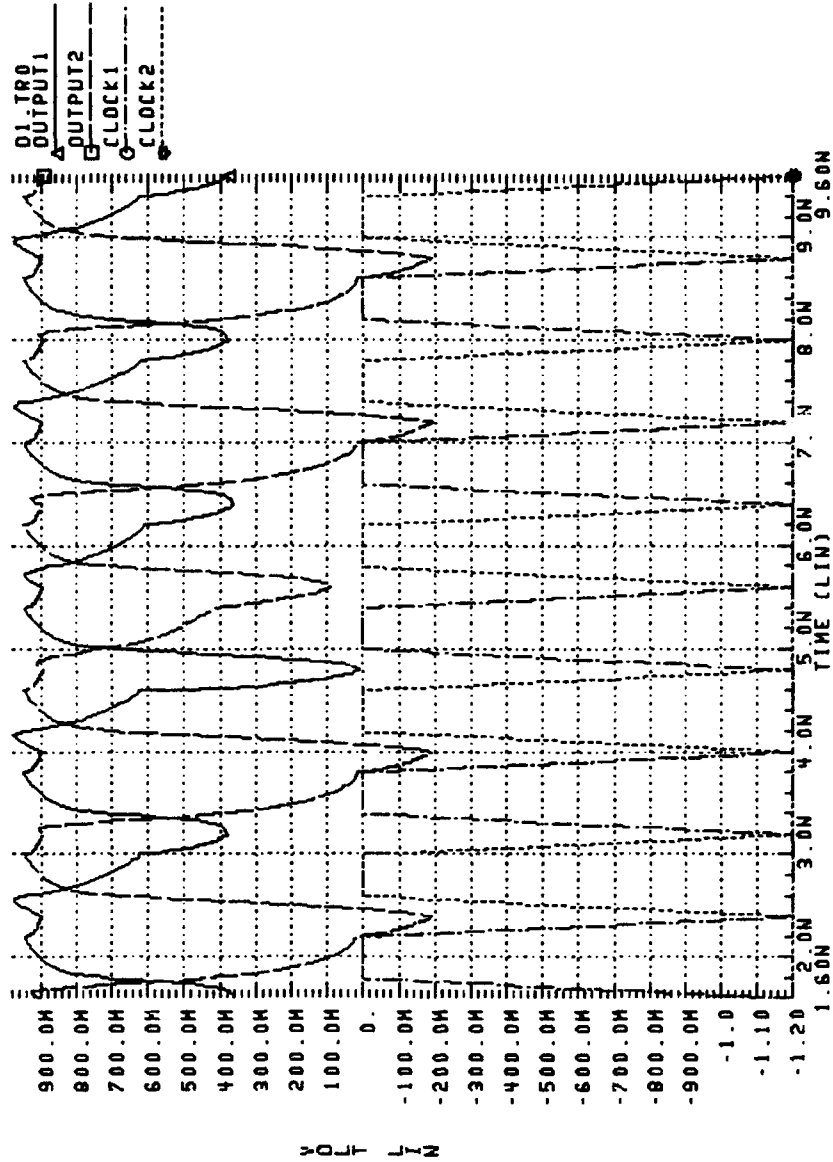
VITESSE H6AAS2 TDFL INVERTER SEU SIM FOR DB (.74 MA SRC TO DRAIN)  
26-JUL93 18:12:37



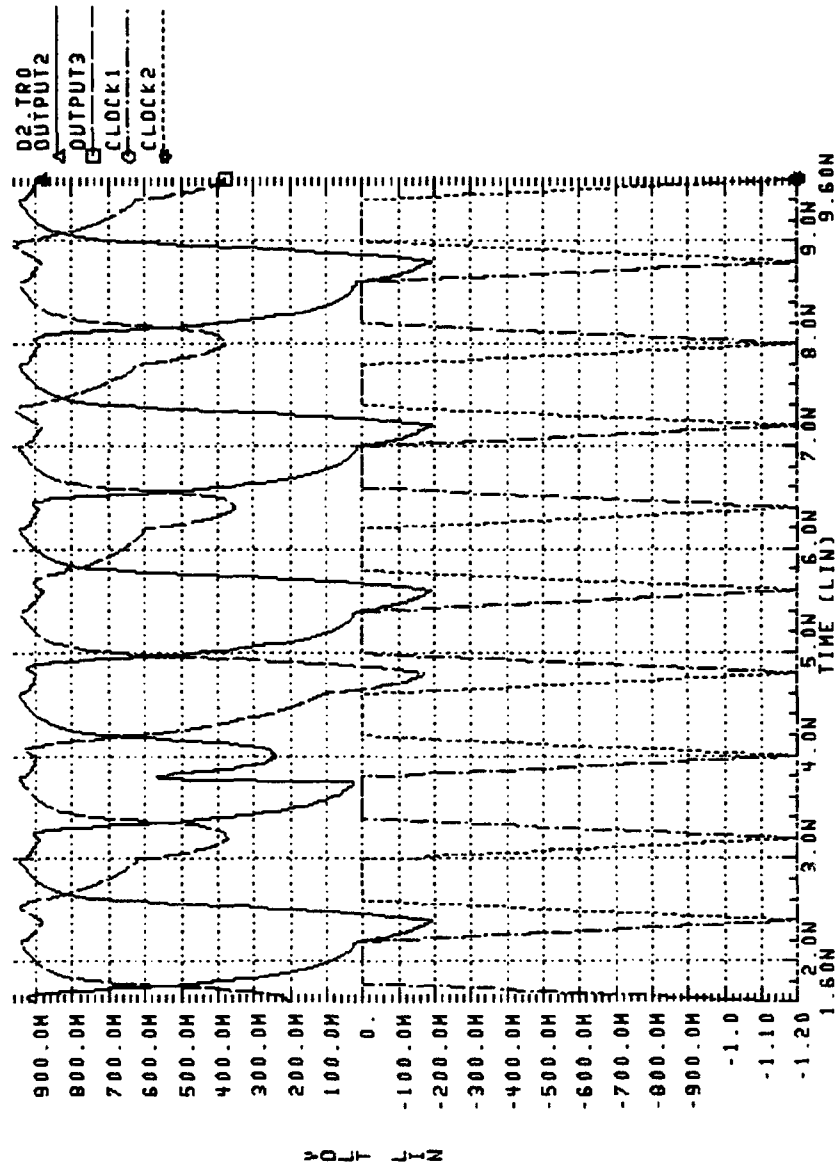
VITESSE HGARS2 TOFL INVERTER SEU SIM FOR DB (.085 NA SRC TO GATE)  
27-JUL93 15:37:53



VITESSE HGAAS2 TOFL INVERTER SEU SIM FOR D11 (.175 MA)  
27-JUL93 16:34:36

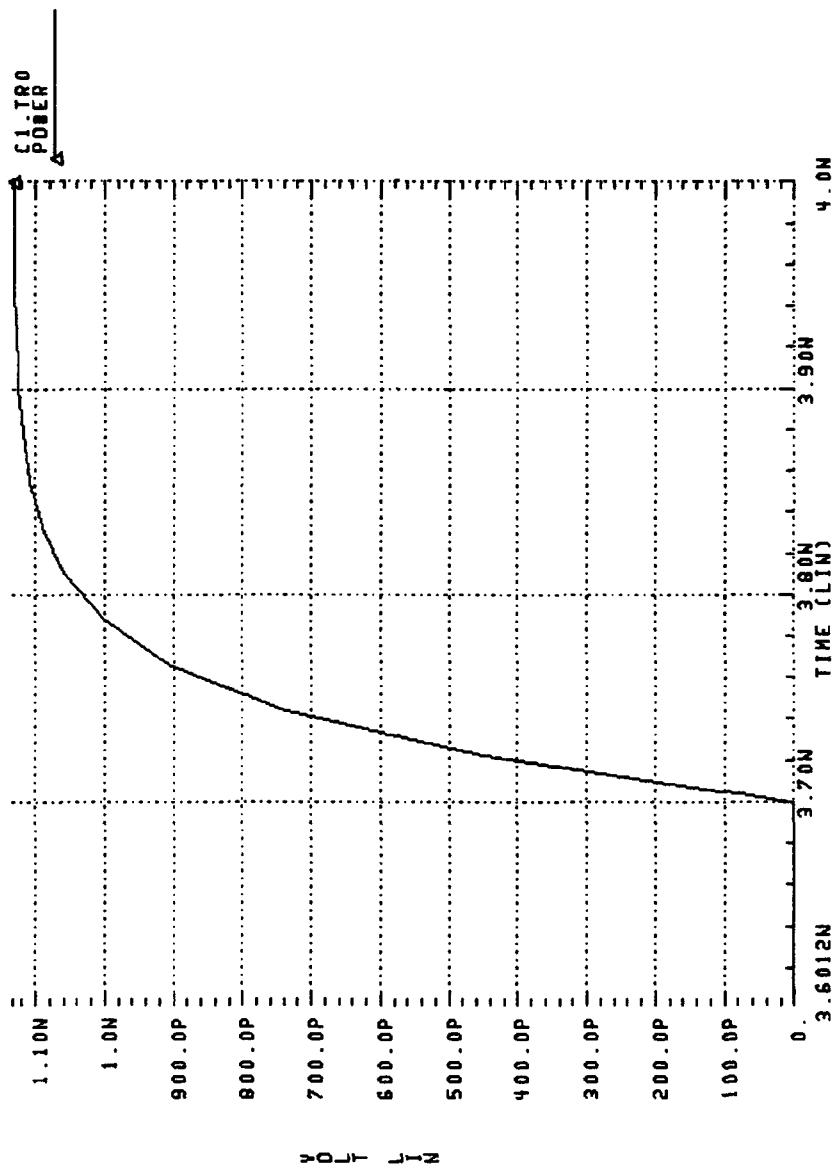


YITESSE HGARS2 TOFL INVERTER SED SIM FOR DI2 (.535 NA)  
27-JUL93 17:25:55

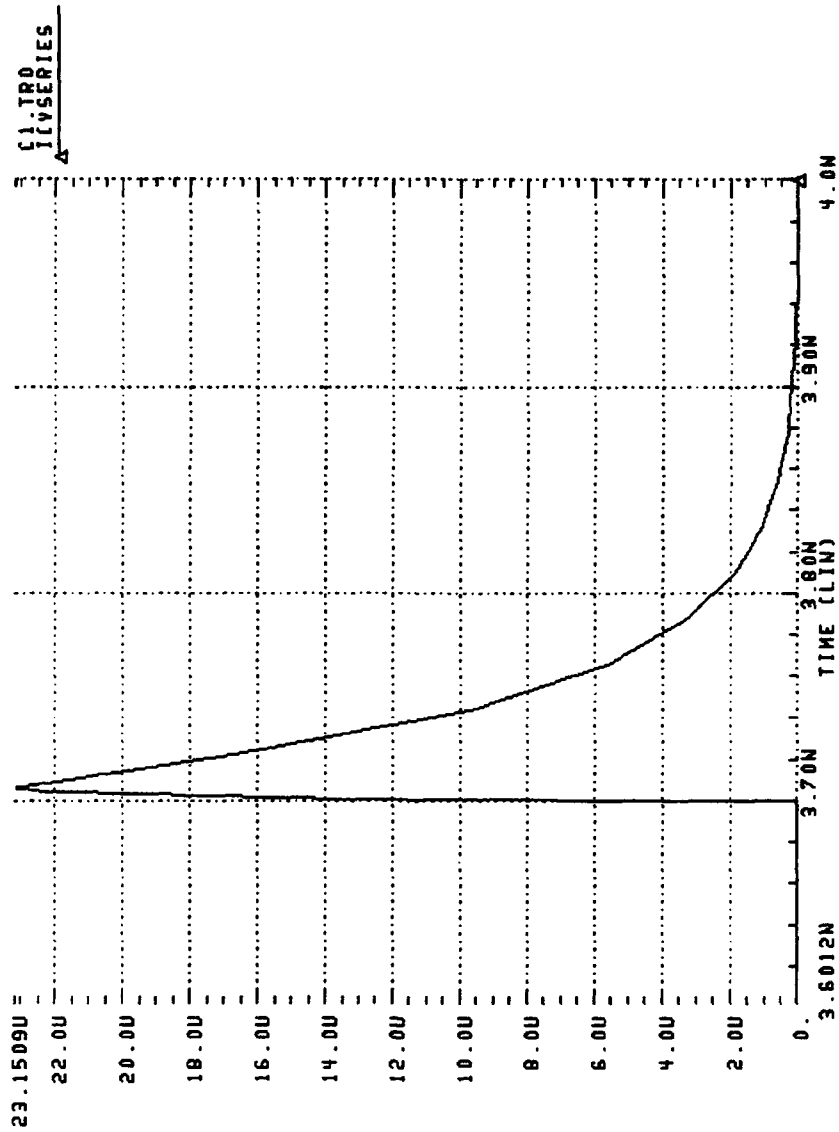


CHARGE REQUIRED TO PRECIPITATE A SEU OF TRANSISTOR D1 (SRC TO DRAIN)

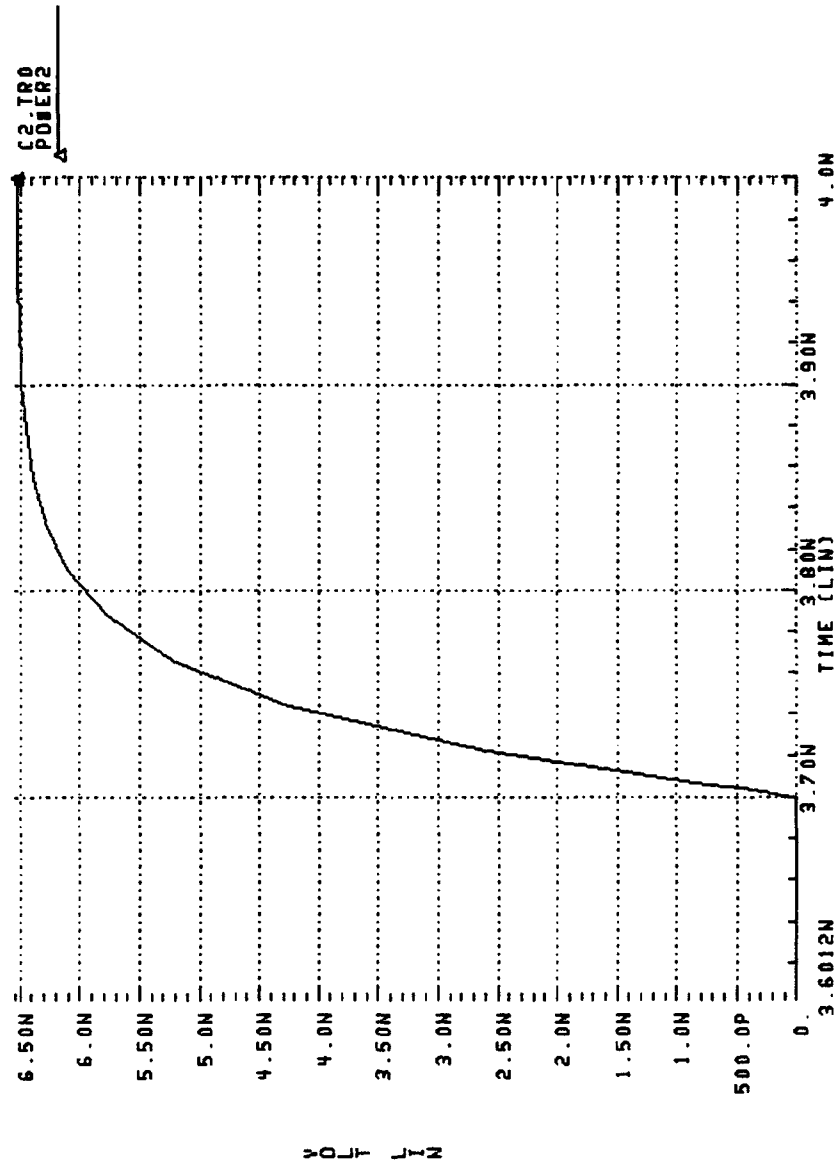
19-JUL-93 15:38:21



CHARGE REQUIRED TO PRECIPITATE A SEU OF TRANSISTOR 01 (SRC TO DRAIN)  
19-JUL93 15:38:21



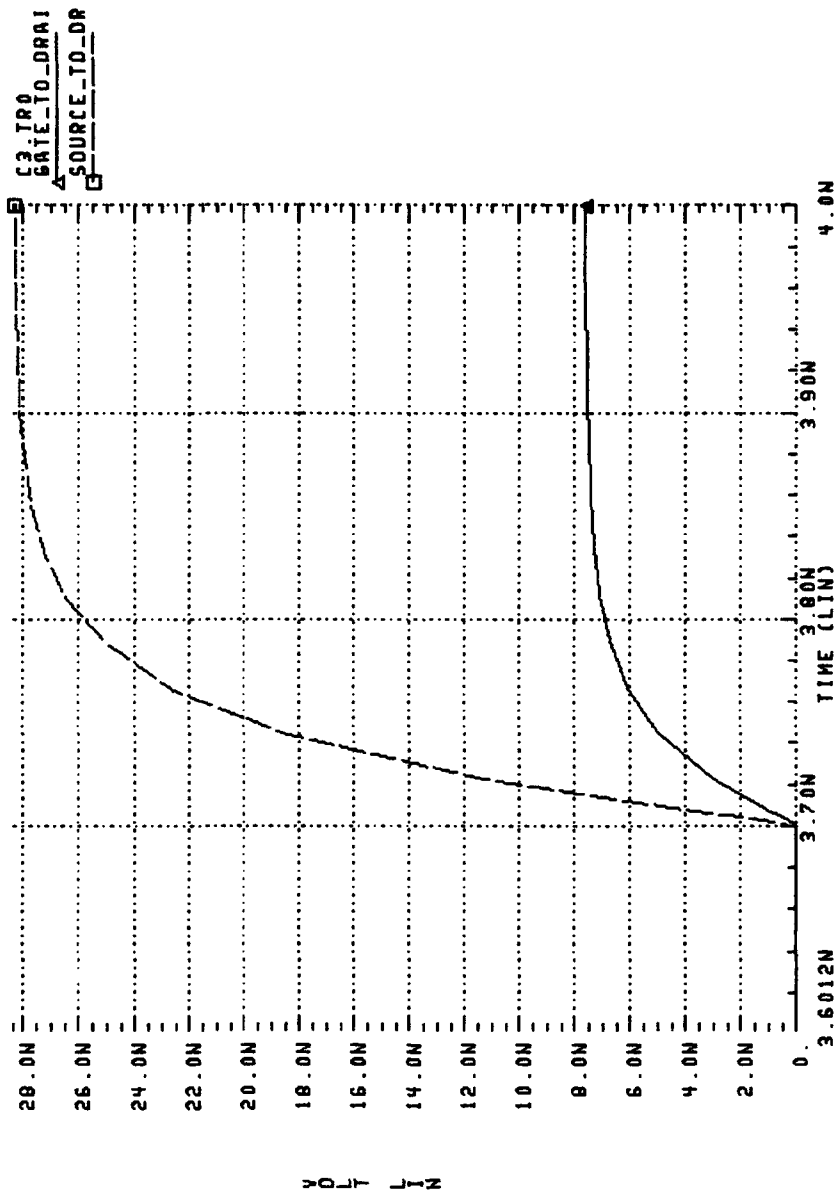
CHARGE REQUIRED TO PRECIPITATE A SEU OF TRANSISTOR 02 (SRC TO DRAIN)  
19-JUL93 15:36:27





CHARGE REQUIRED TO PRECIPITATE A SEU OF TRANSISTOR 03 (COMPARISON PLOT)

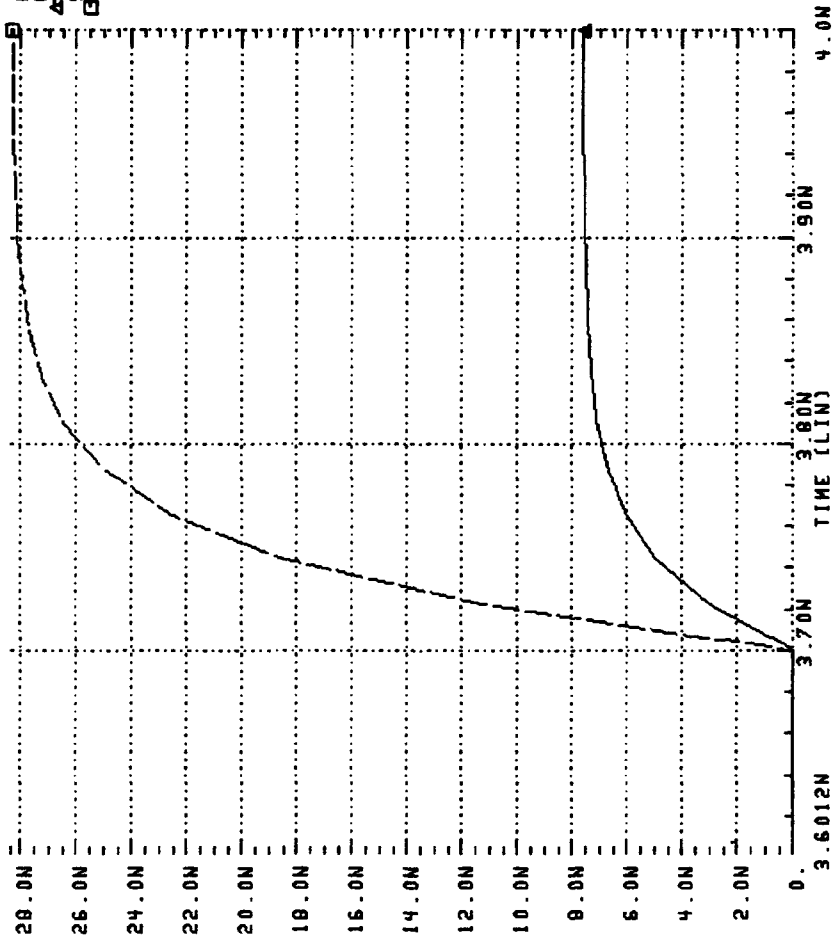
19-JUL-93 16:54:34



CHARGE REQUIRED TO PRECIPITATE A SEU OF TRANSISTOR 03 (COMPARISON PLOT)

19-JUL-93 18:54:34

C3.TRO  
A GATE\_TO\_DRAI  
B SOURCE\_IO\_DR

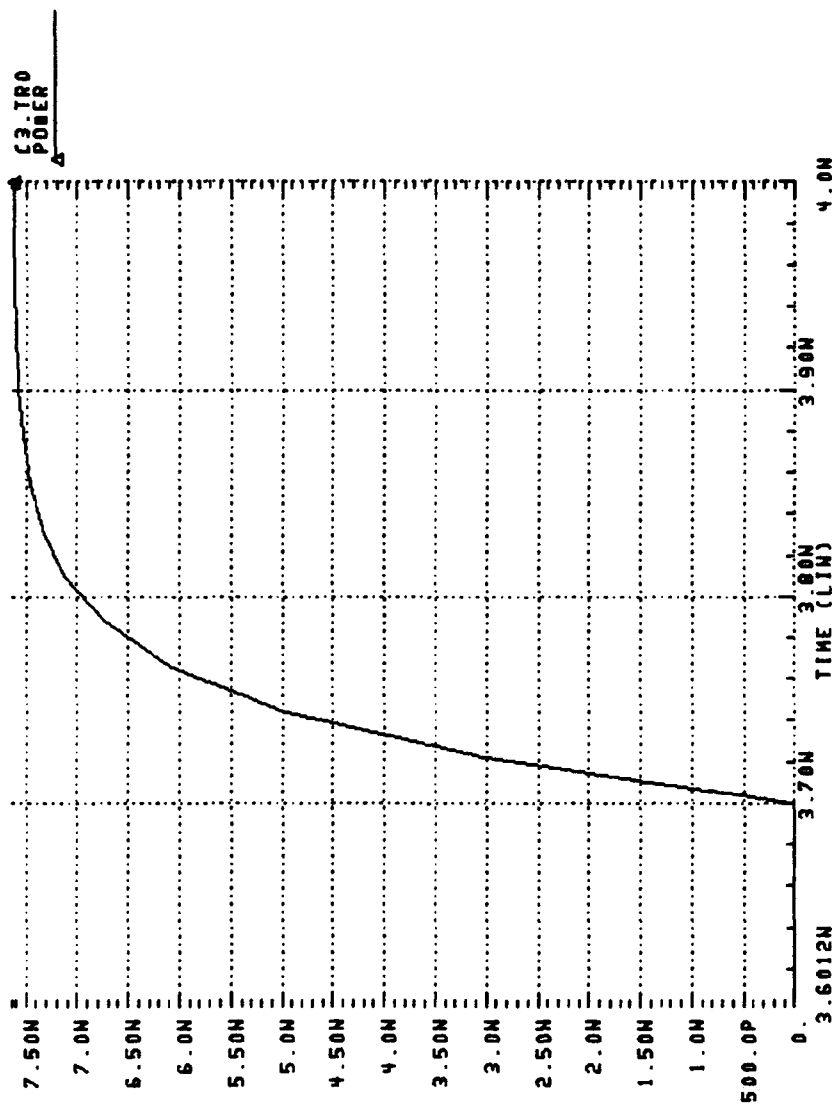


VOLT

TIME

CHARGE REQUIRED TO PRECIPITATE A SEU OF TRANSISTOR 03 (GATE TO DRAIN)

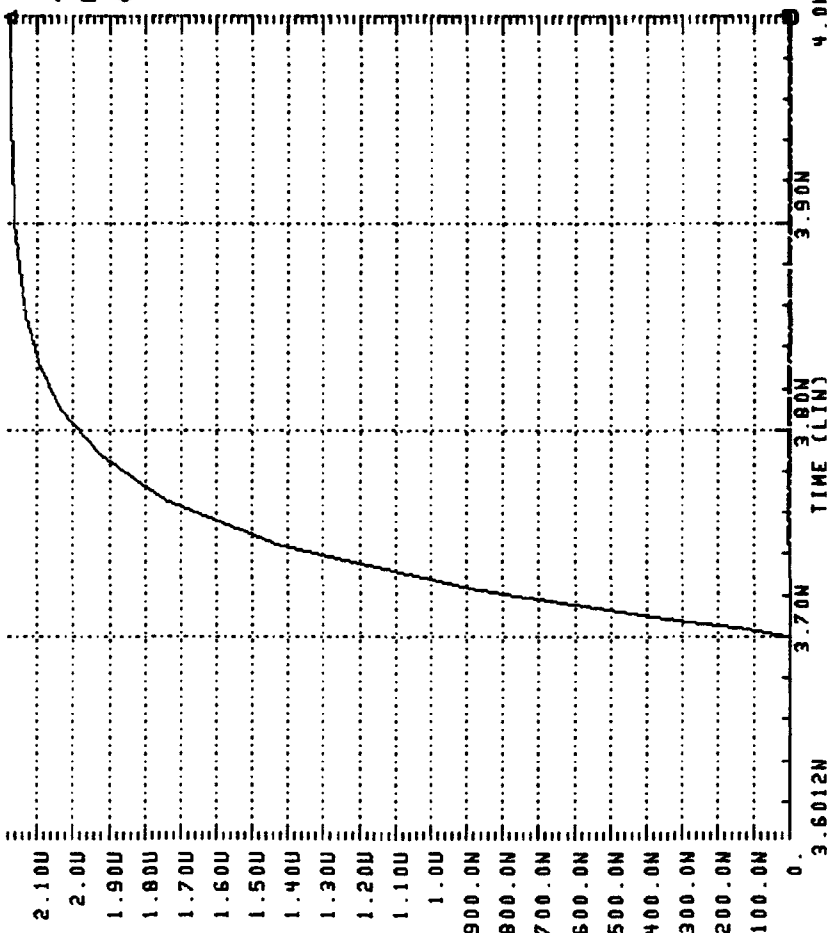
19-JUL-93 15:52:29



# CHARGE REQUIRED TO PRECIPITATE A SEU OF TRANSISTOR 04 (COMPARISON PLOT)

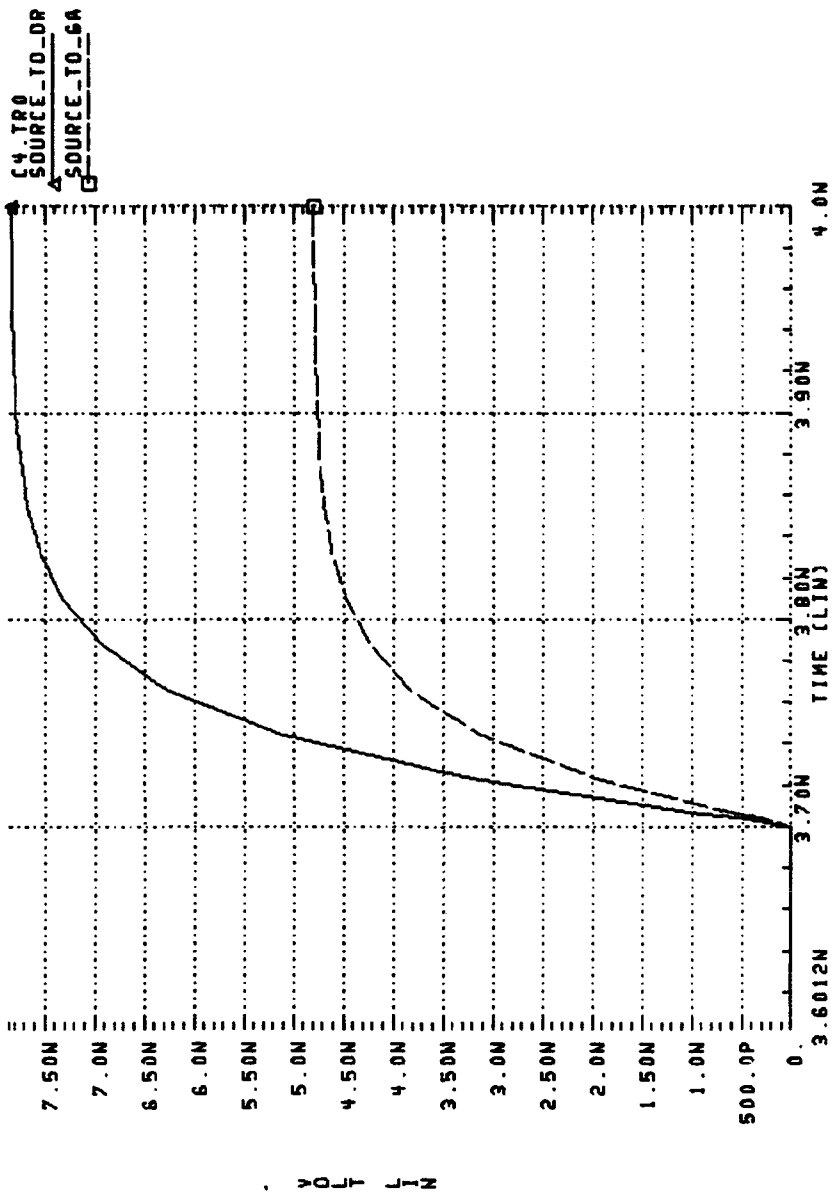
19-JUL-93 16:45:25

CH TR0  
GATE\_TO\_DRAI  
SOURCE\_TO\_DR  
SOURCE\_TO\_GA



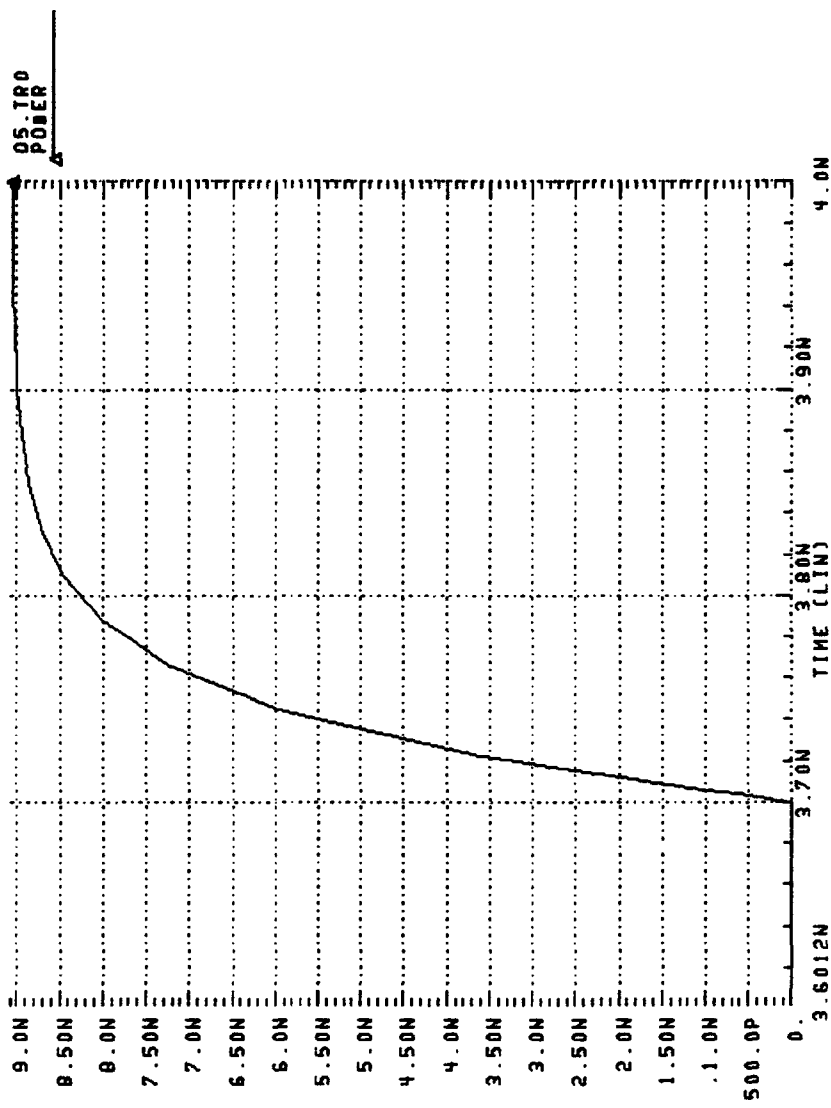
70 1 1 N

CHARGE REQUIRED TO PRECIPITATE A SEU OF TRANSISTOR 04 (COMPARISON PLOT)  
19-JUL93 16:45:25



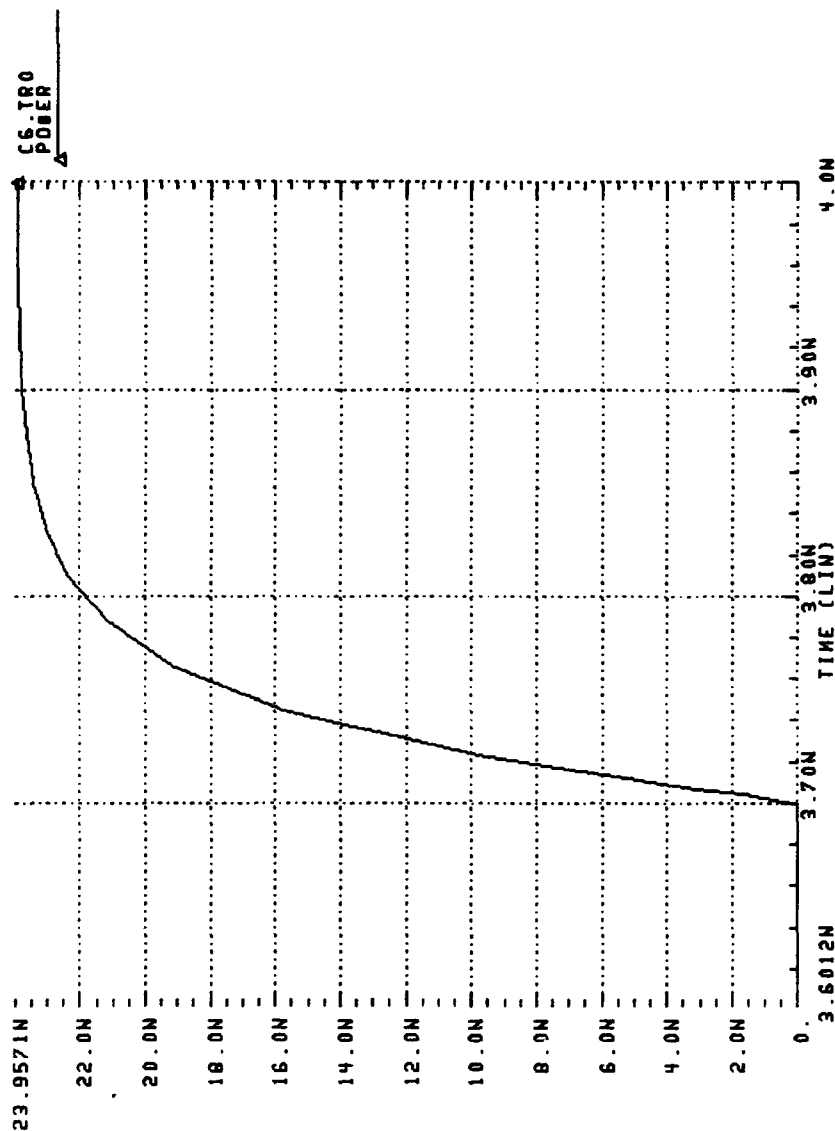
CHARGE REQUIRED TO PRECIPITATE A SEU OF TRANSISTOR 05 (GATE TO SOURCE)

22-JUL93 15:41:38

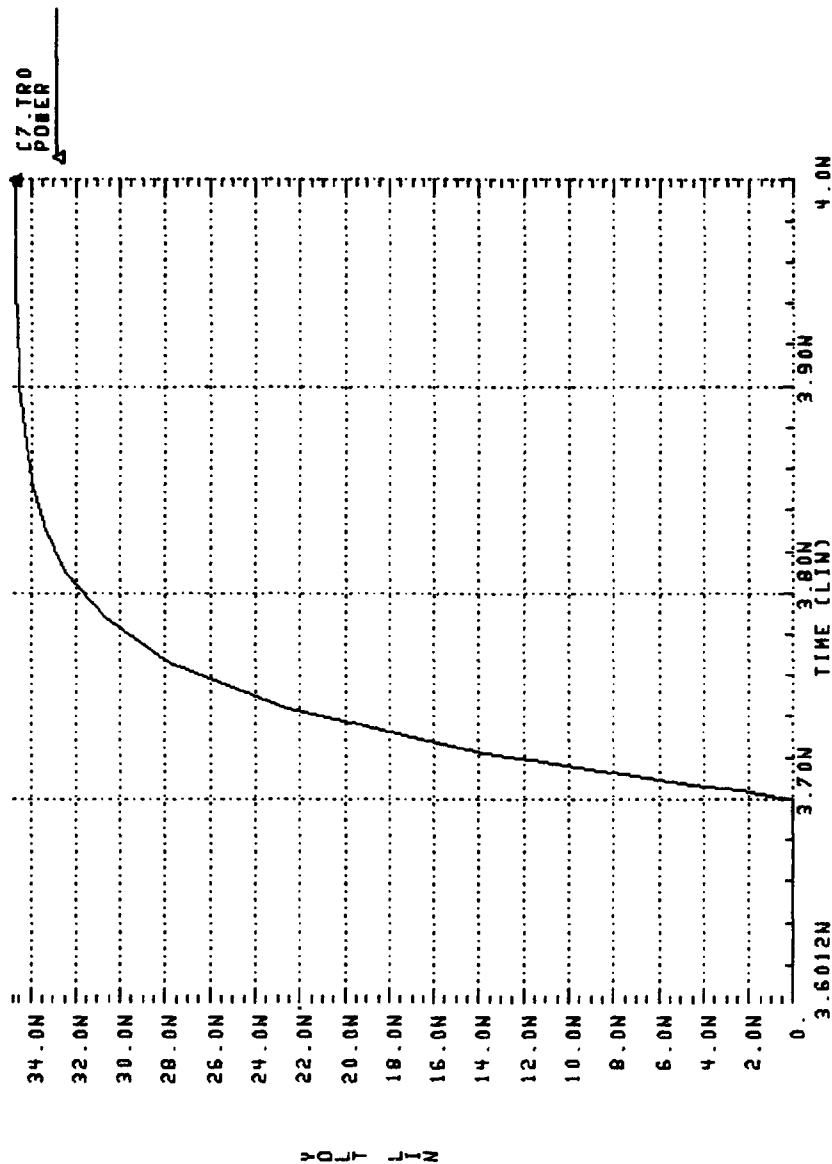


CHARGE REQUIRED TO PRECIPITATE A SEU OF TRANSISTOR 06 (SRC TO DRAIN)

19 JUL 93 17: 8:40

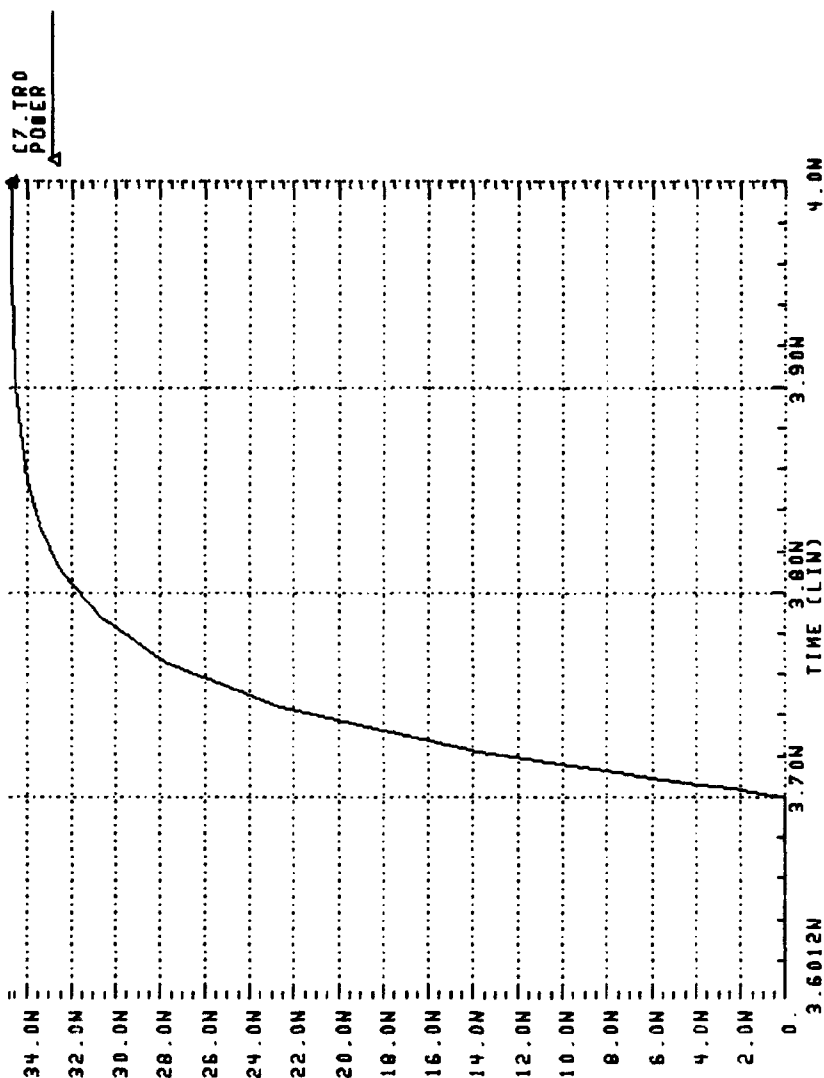


CHARGE REQUIRED TO PRECIPITATE A SEU OF TRANSISTOR 07 (SRC TO GATE)  
26-JUL93 17:30:12



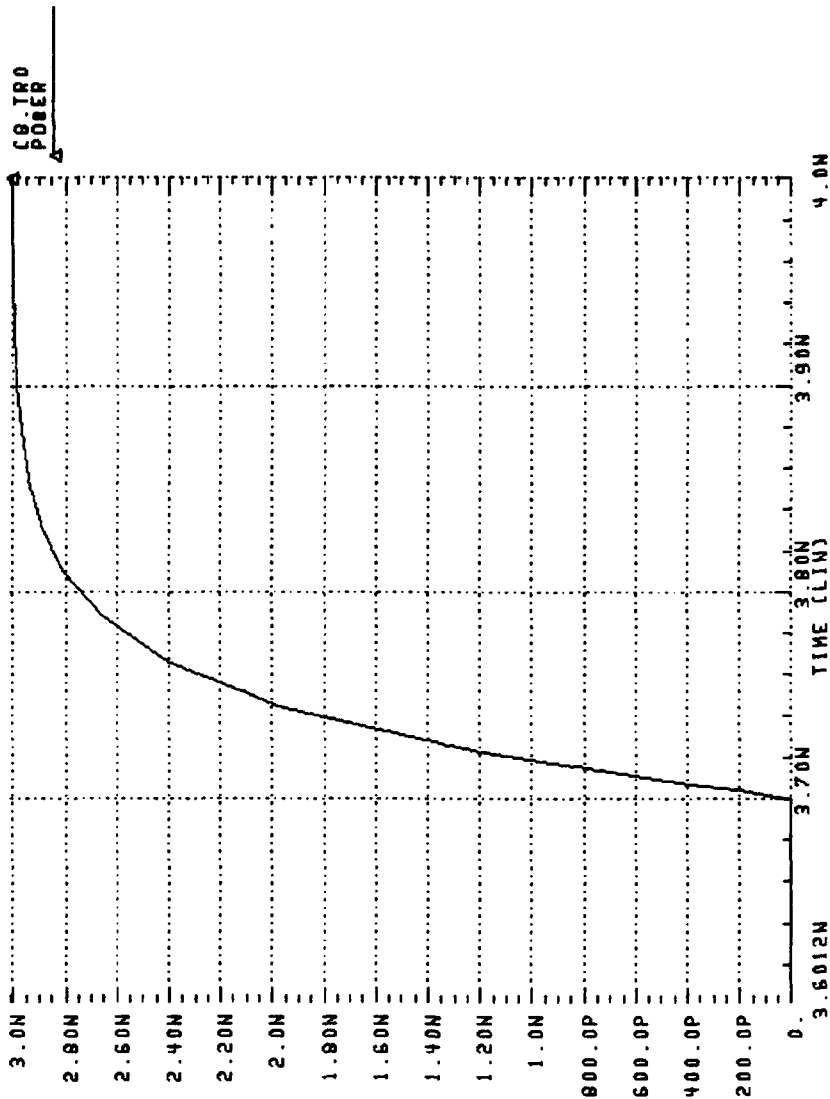


CHARGE REQUIRED TO PRECIPITATE A SFU OF TRANSISTOR 07 (SRC TO GATE)  
26-JUL-93 17:30:12

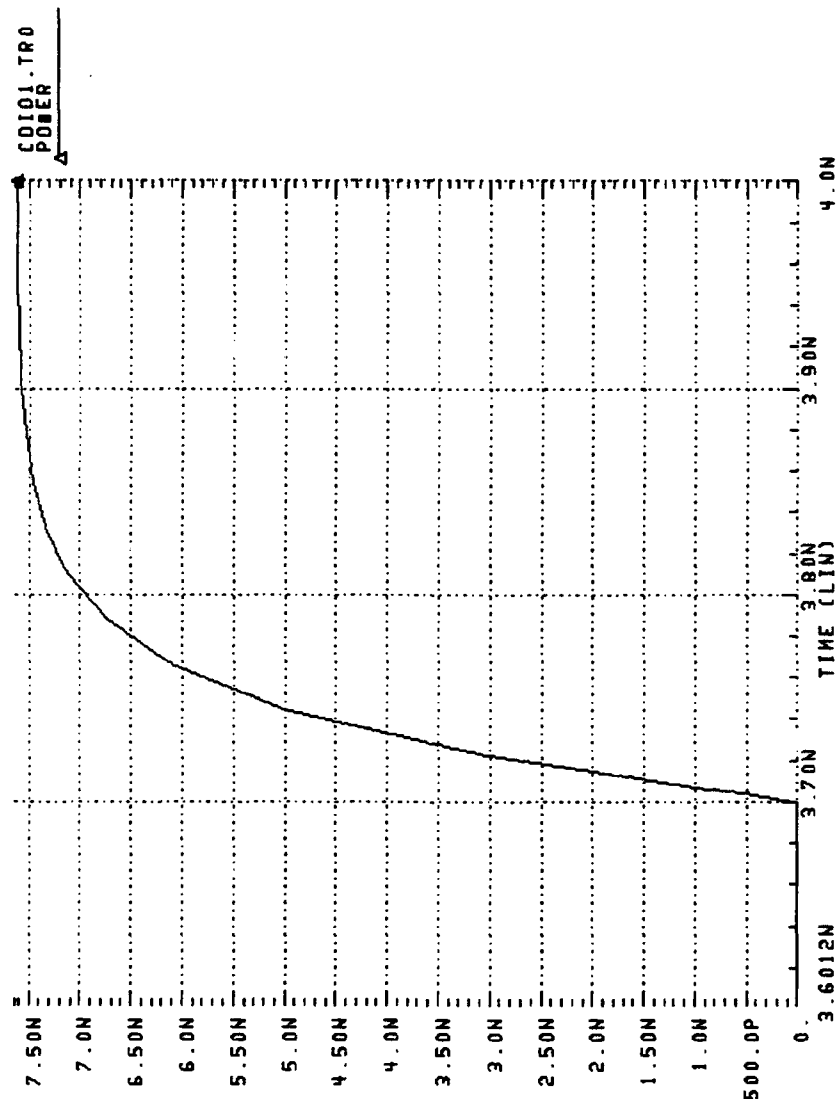


NO L T N

CHARGE REQUIRED TO PRECIPITATE A SEU OF TRANSISTOR 08 (SRC TO DRAIN)  
27 JUL 93 16:10: 5

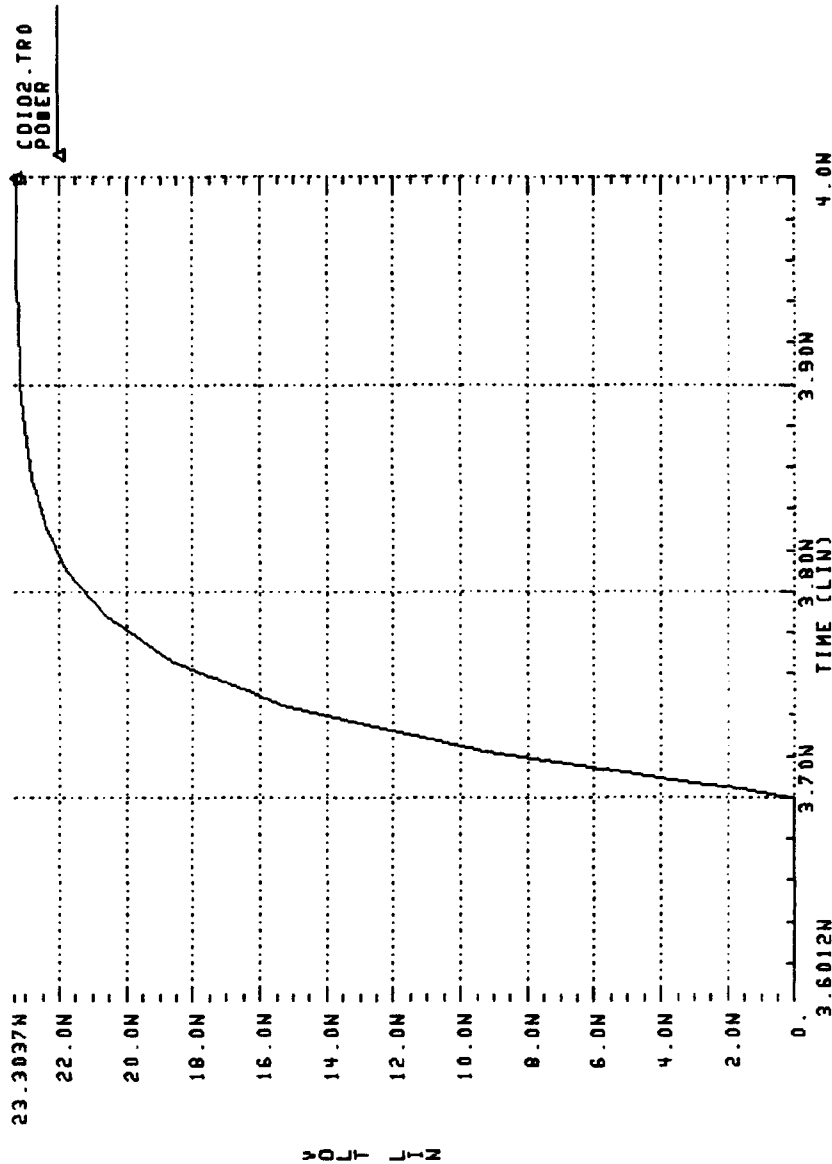


CHARGE REQUIRED TO PRECIPITATE A SEU OF DIODE1  
27 JUL93 17:20:46



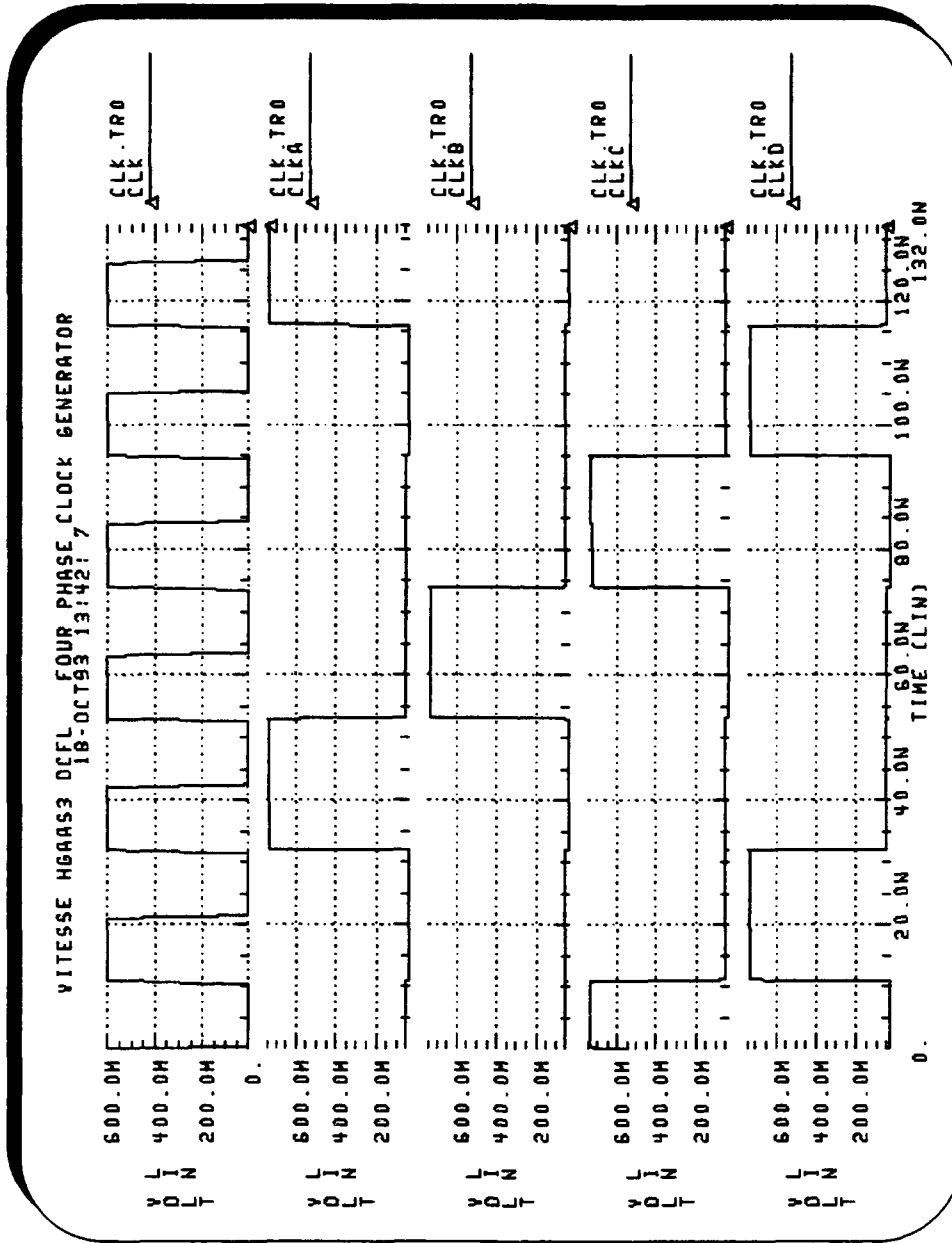
# CHARGE REQUIRED TO PRECIPITATE A SEU OF DIODE2

27-JUL93 17:18:30

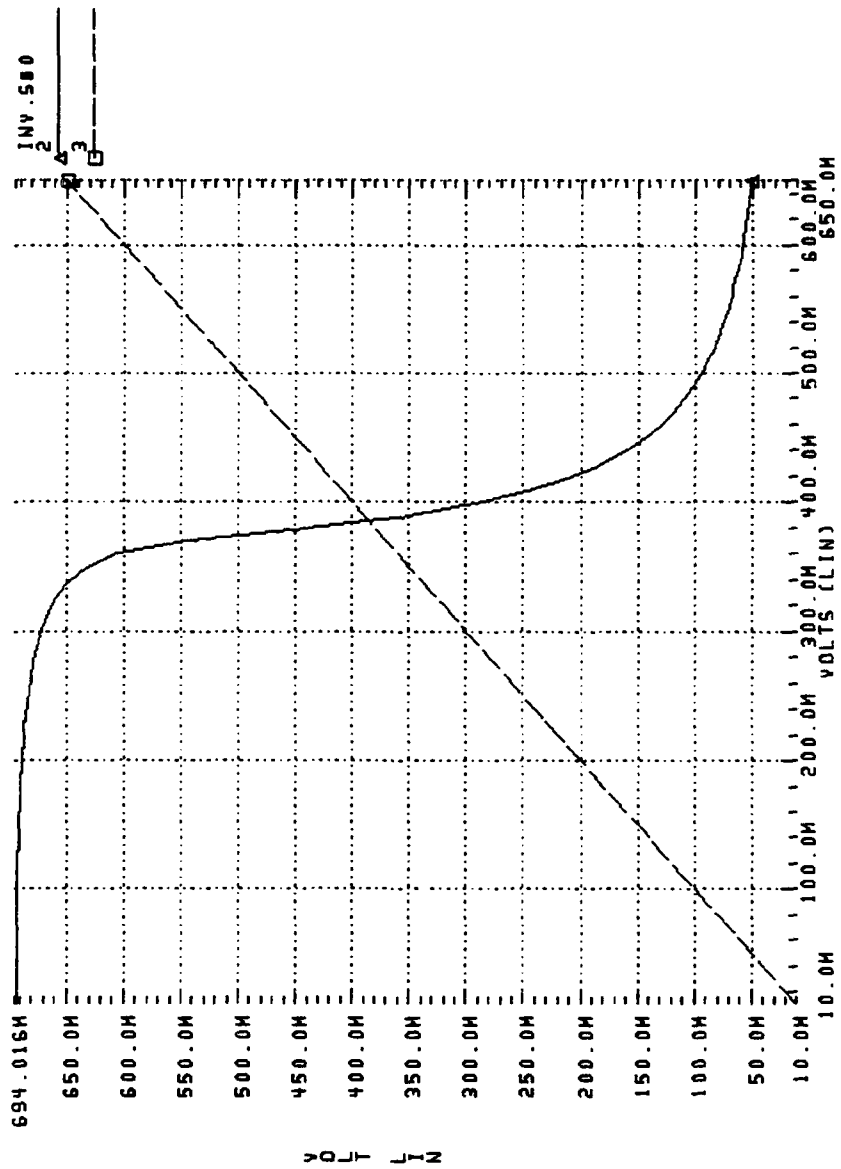


# APPENDIX B CHIP VERIFICATION

## SIMULATIONS

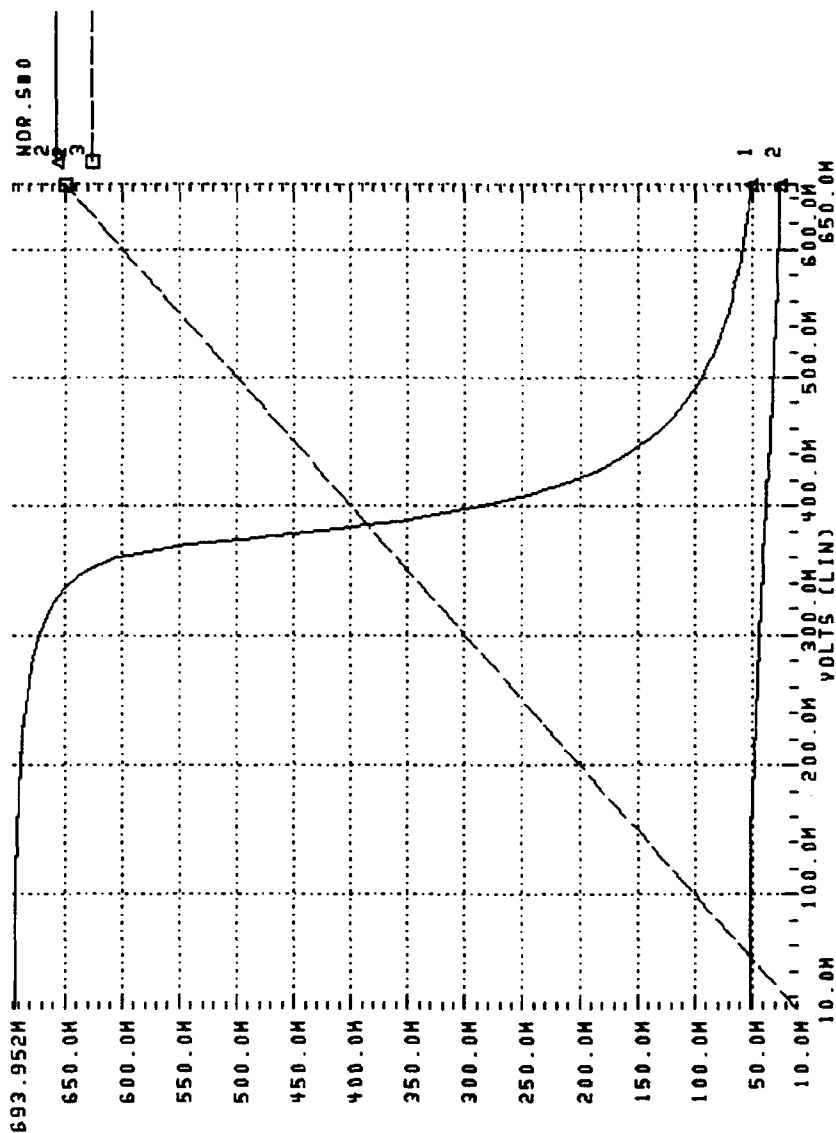


VITESSE H6AAS3 DCFL INVERTER (DC ANALYSIS)  
18-OCT93 12:59:50

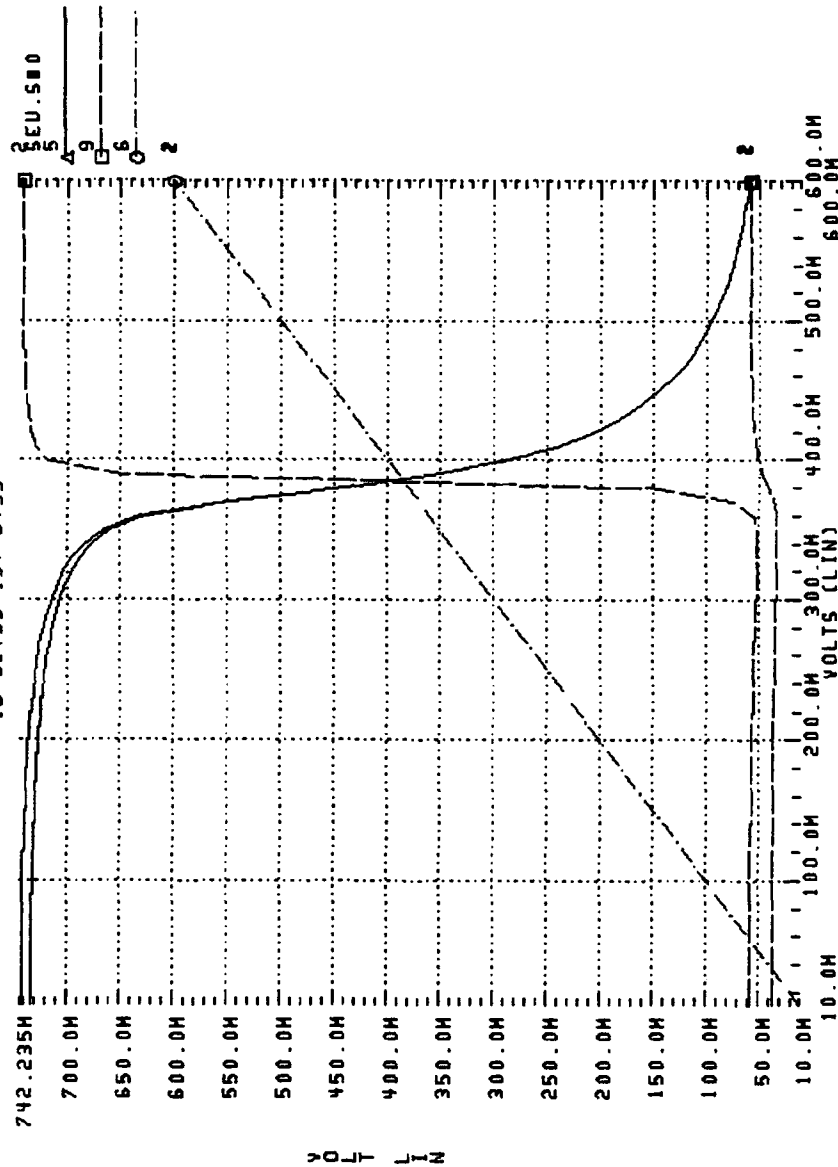


VITESSE H6AAS3 DCFL NOR GATE (DC ANALYSIS)

18-DEC-93 12:57:06

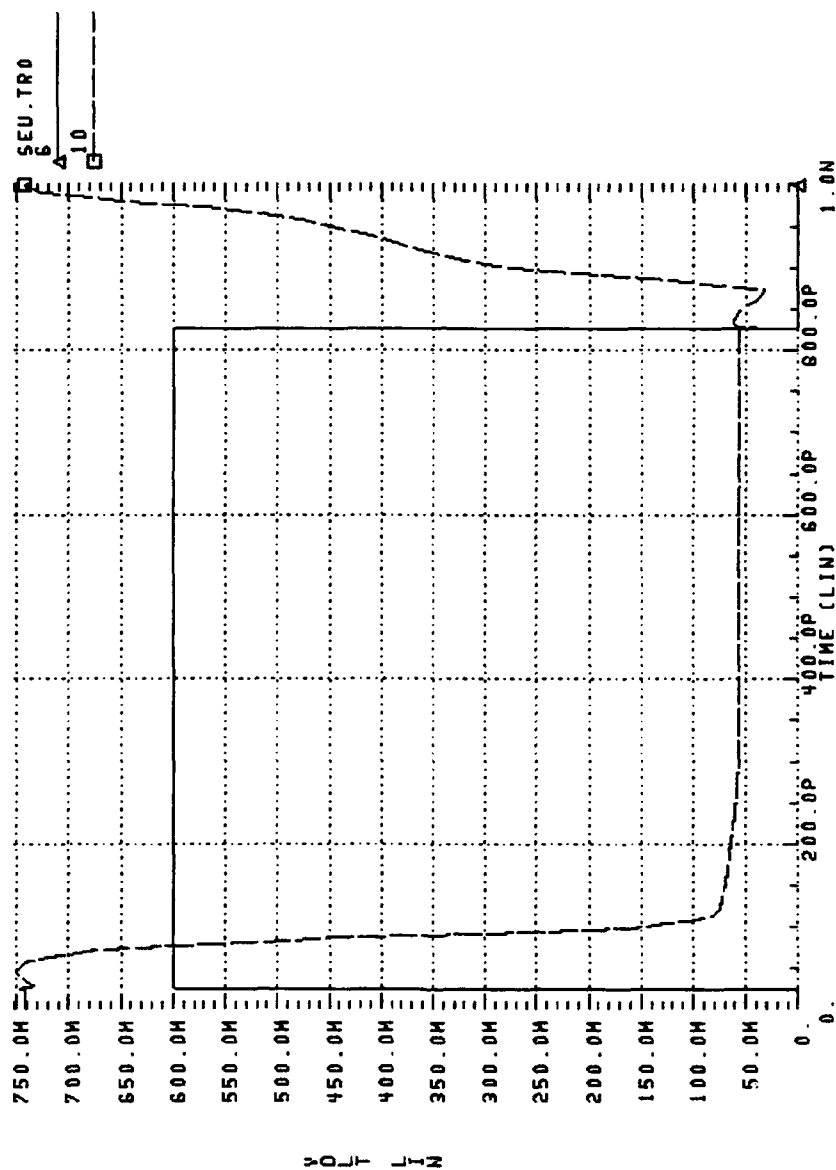


VITESSE HGARS3 DCFL SEU TEST CIRCUIT (DC ANALYSIS)  
18-OCT93 13: 6:59

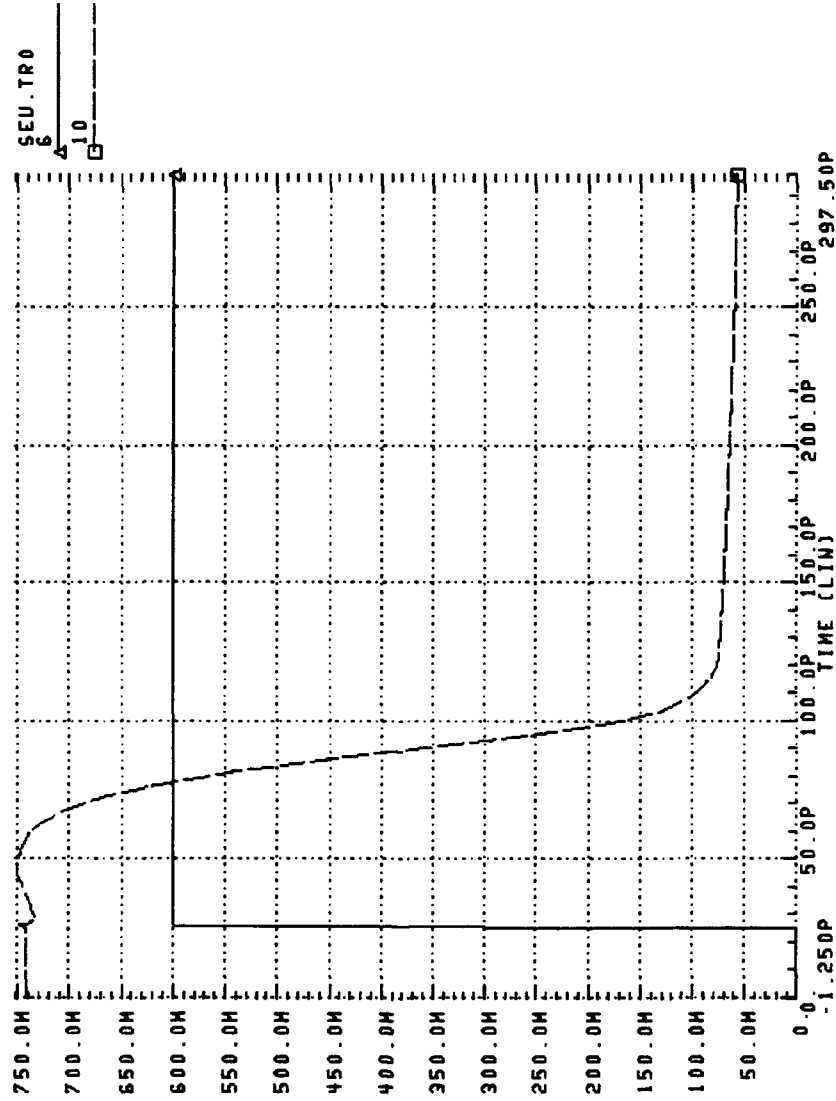




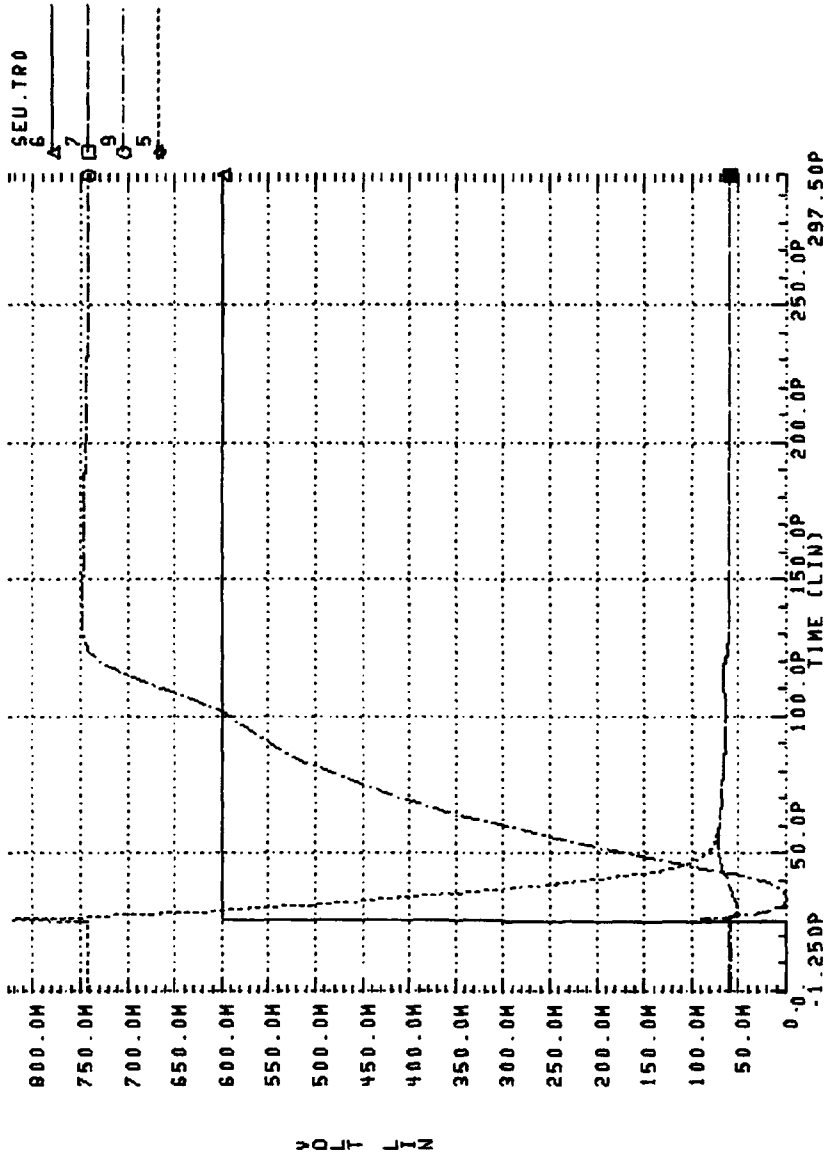
VITESSE H6A953 OCFL SEU TEST CIRCUIT (TRANSIENT ANALYSIS)  
18-OCT93 13:27: 2



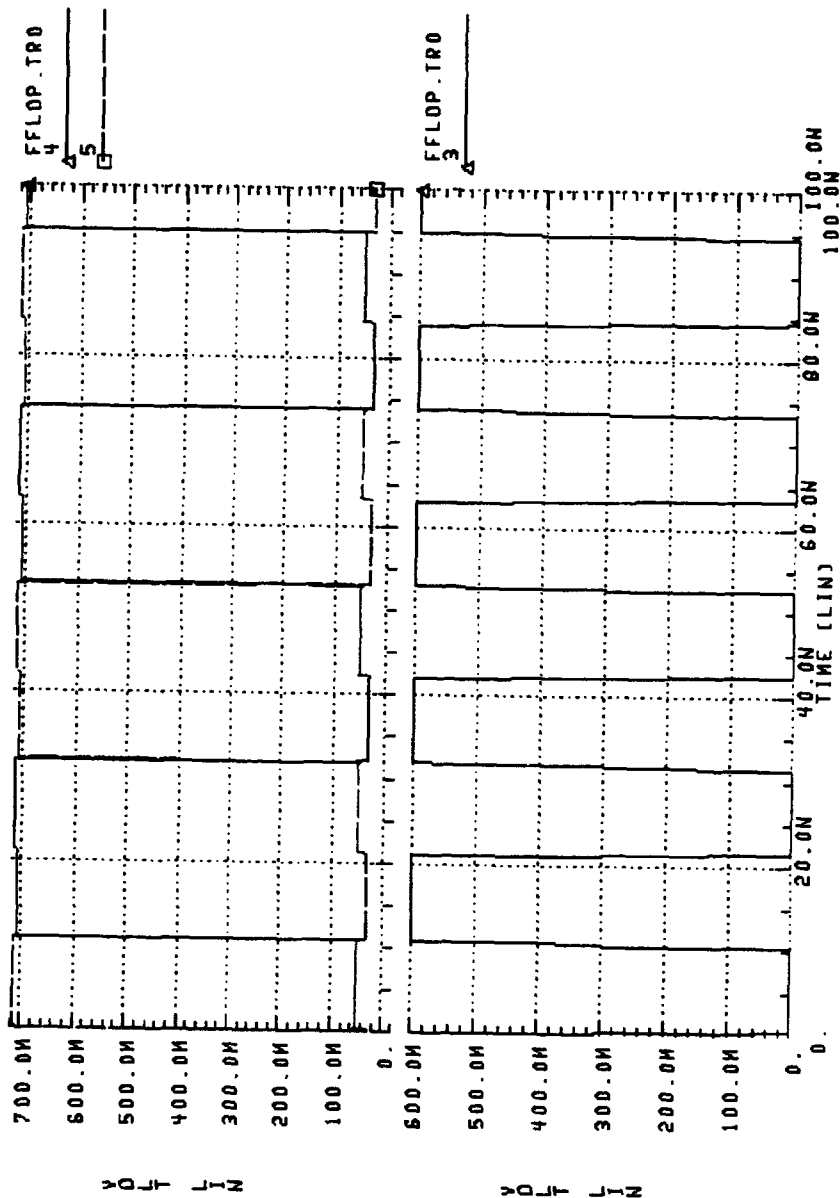
VITESSE HBAAS3 DCFL SEU TEST CIRCUIT (TRANSIENT ANALYSIS)  
18-OCT93 13:27: 2

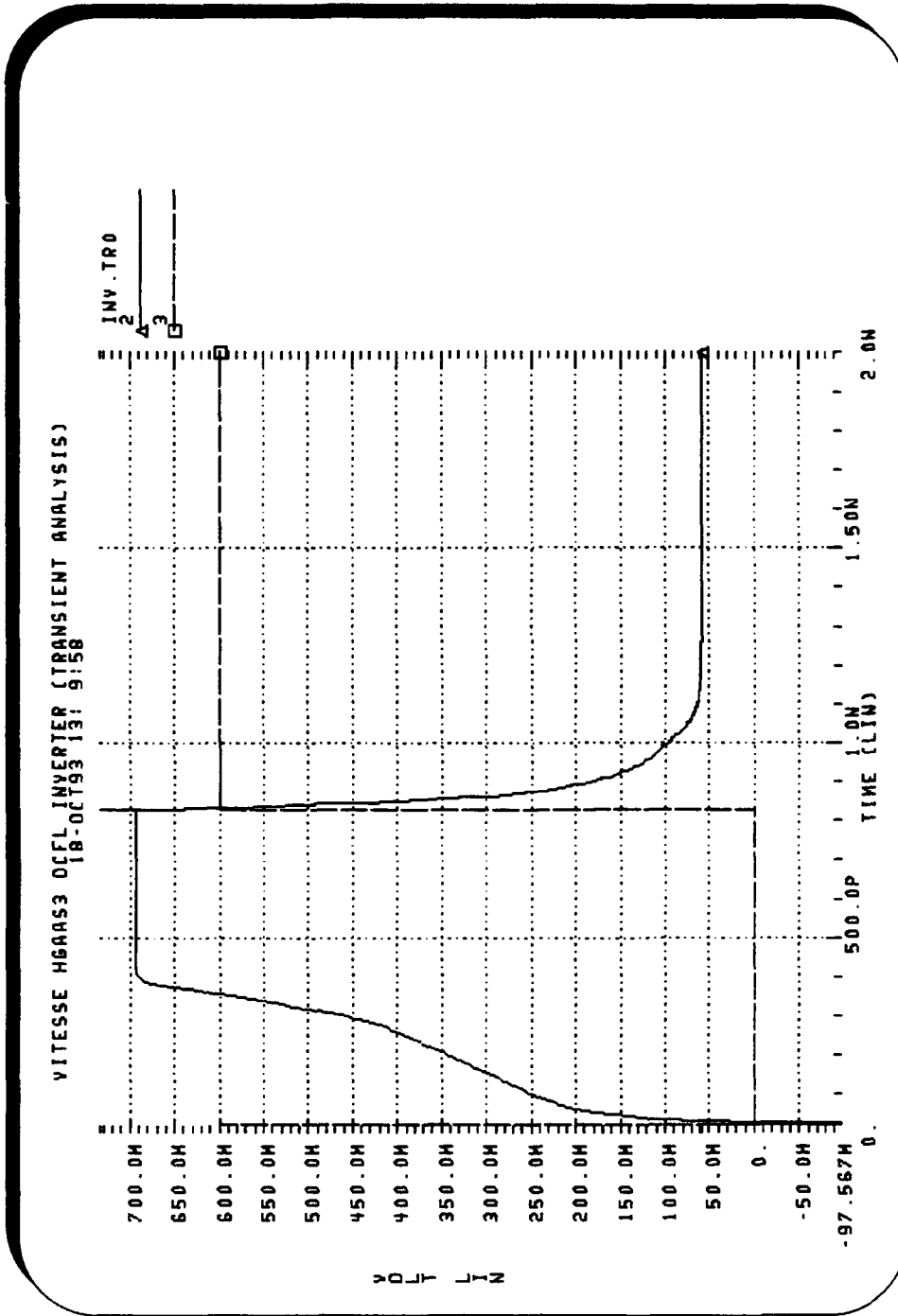


VITESSE HBARS3 DCFL SEU TEST CIRCUIT (TRANSIENT ANALYSIS)  
18-OCT93 13:27: 2

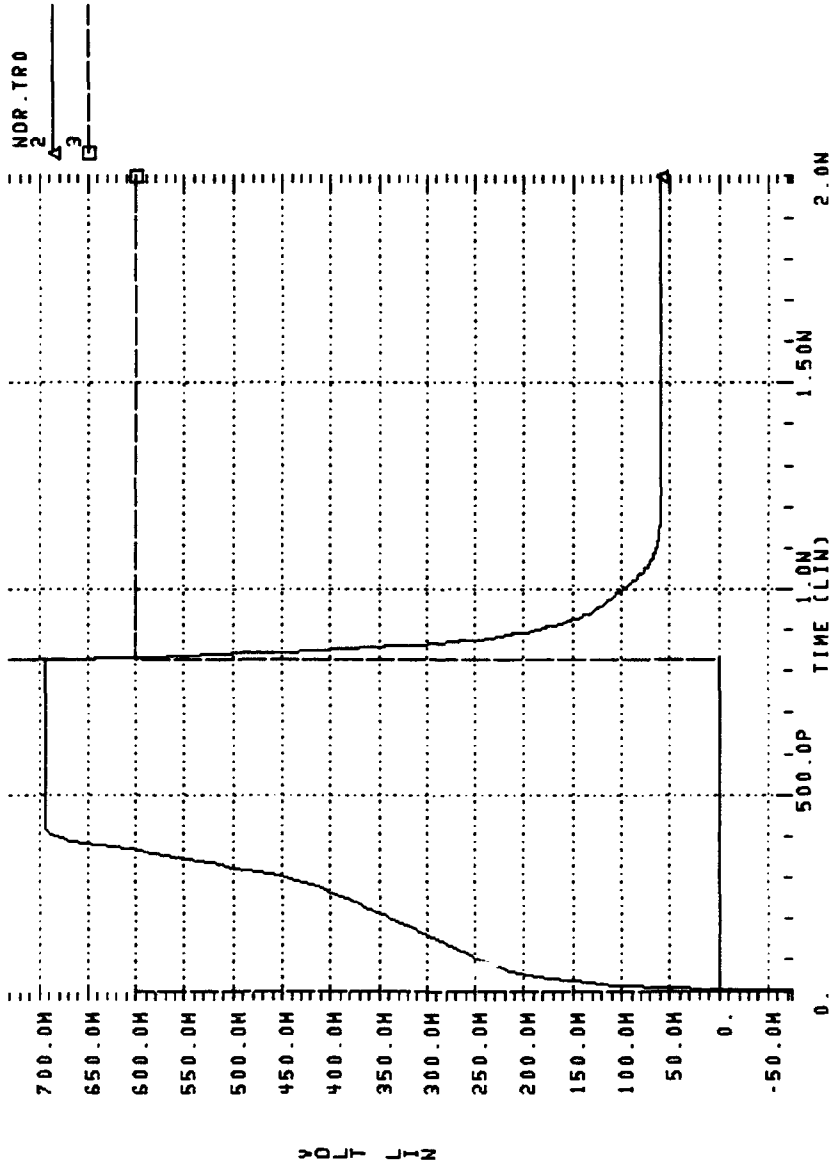


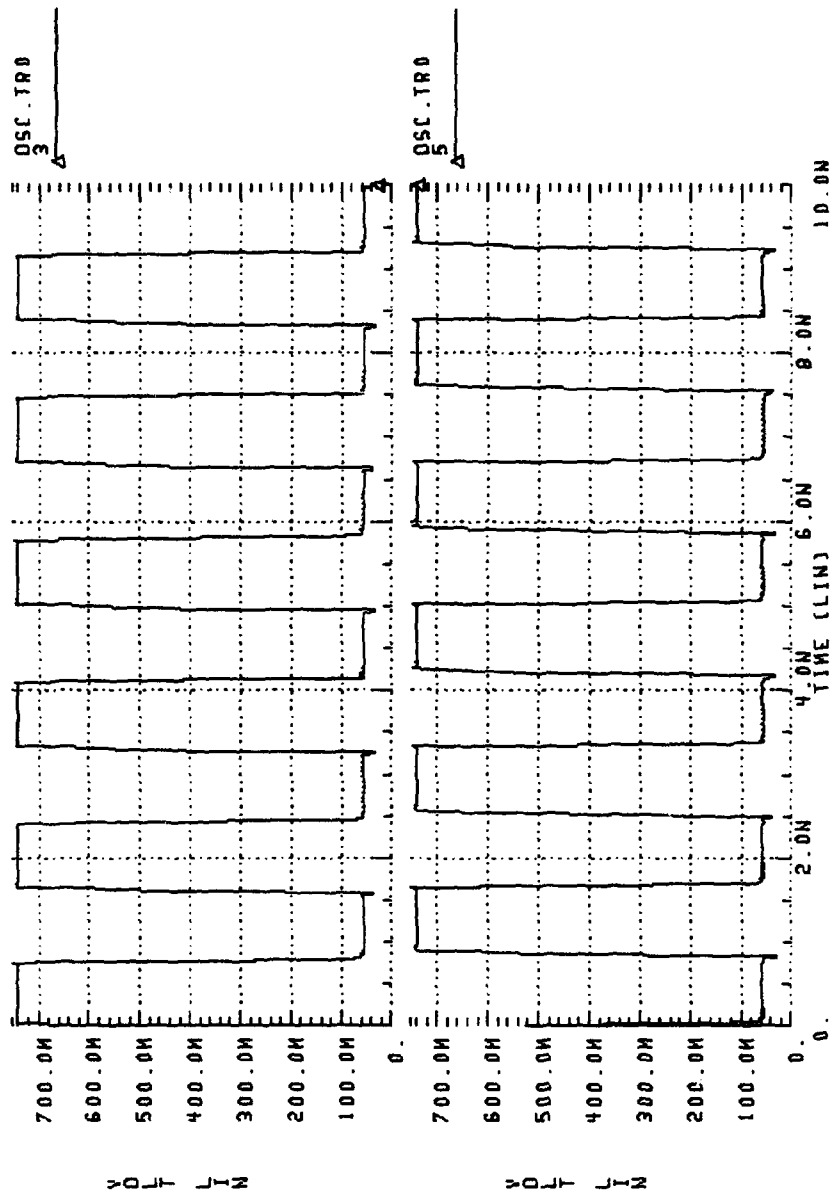
VITESSE H8A953 DCFL FLIP-FLOP  
18-OCT93 13:36:41

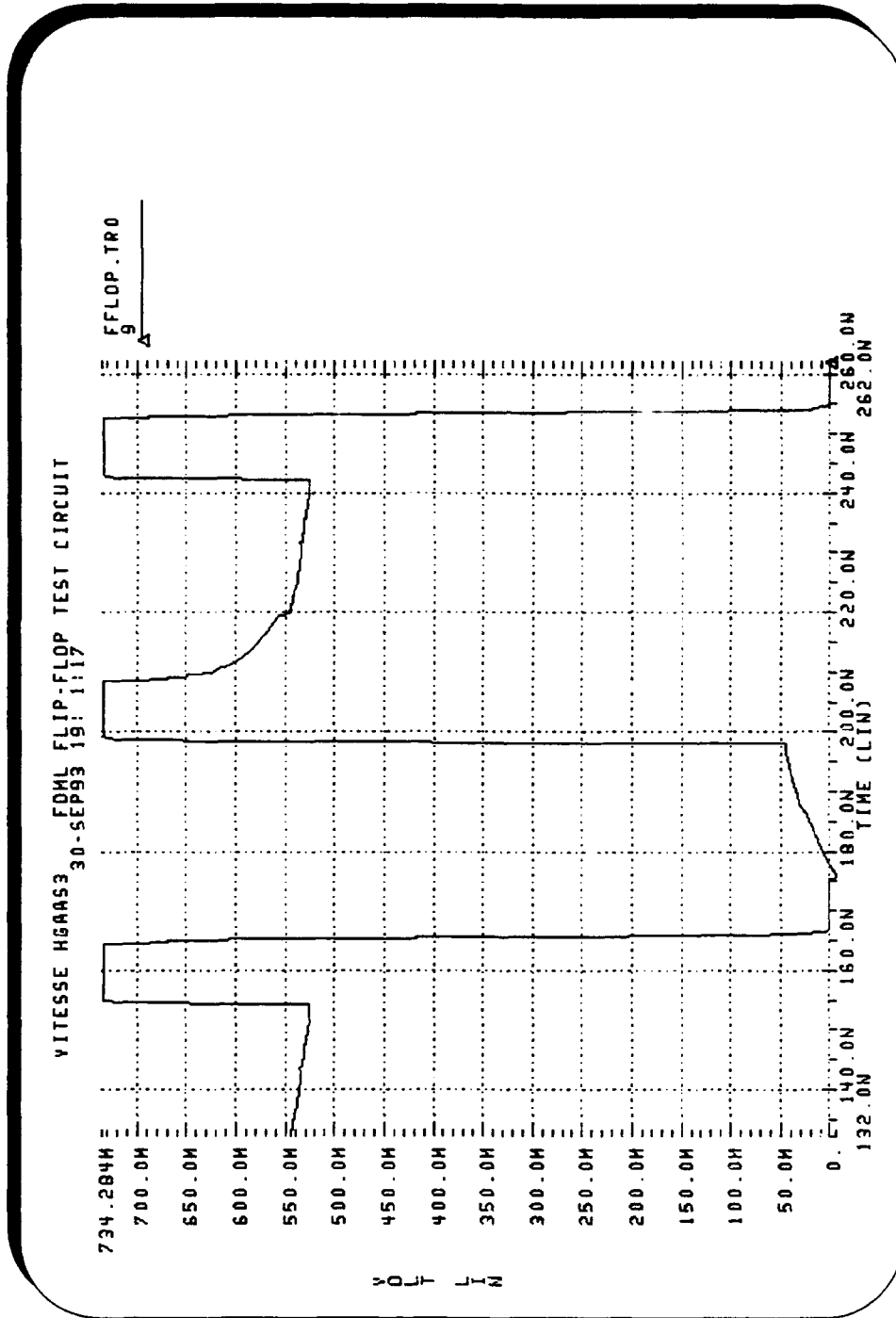




VITESSE HGARS3 DCFL NDR GATE (TRANSIENT ANALYSIS)  
18-OCT93 13:15:13

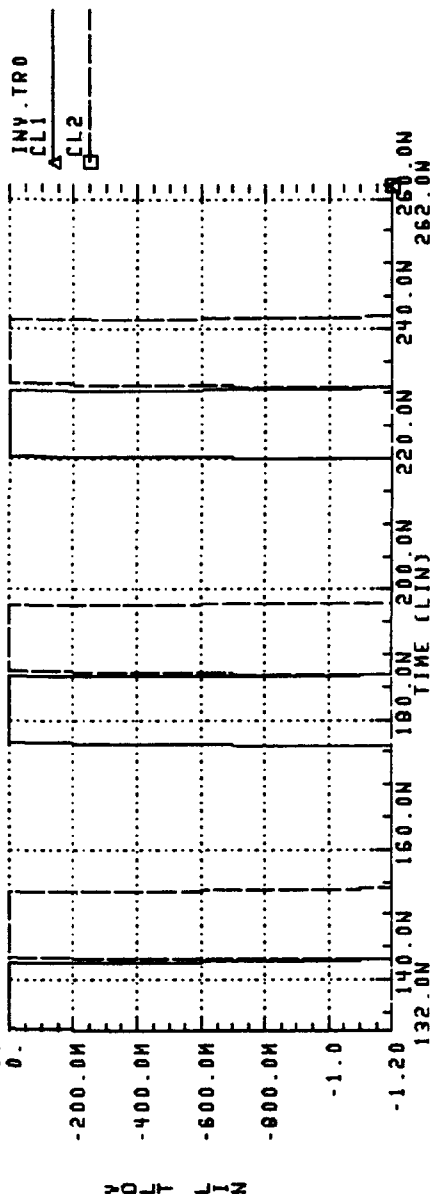
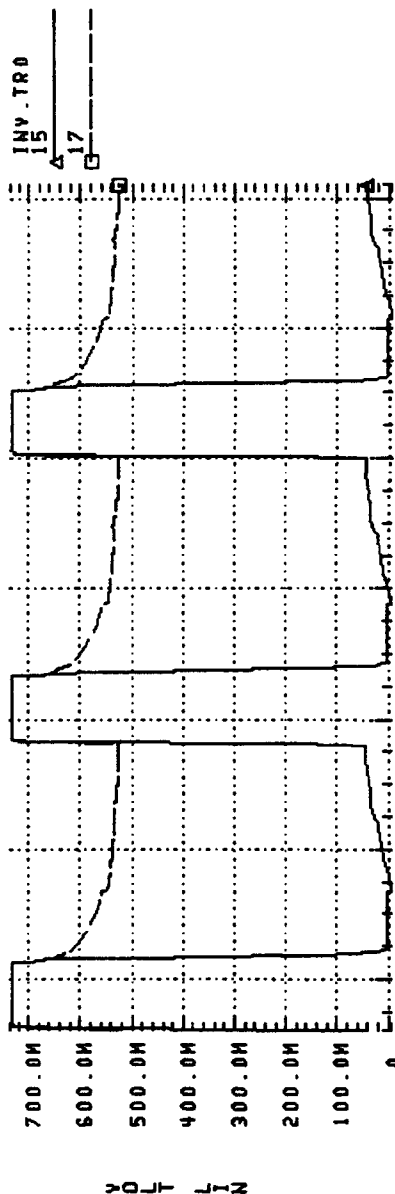


VITESSE HGAAS2 DCFL RING OSCILLATOR  
18-OCT93 13:20:19

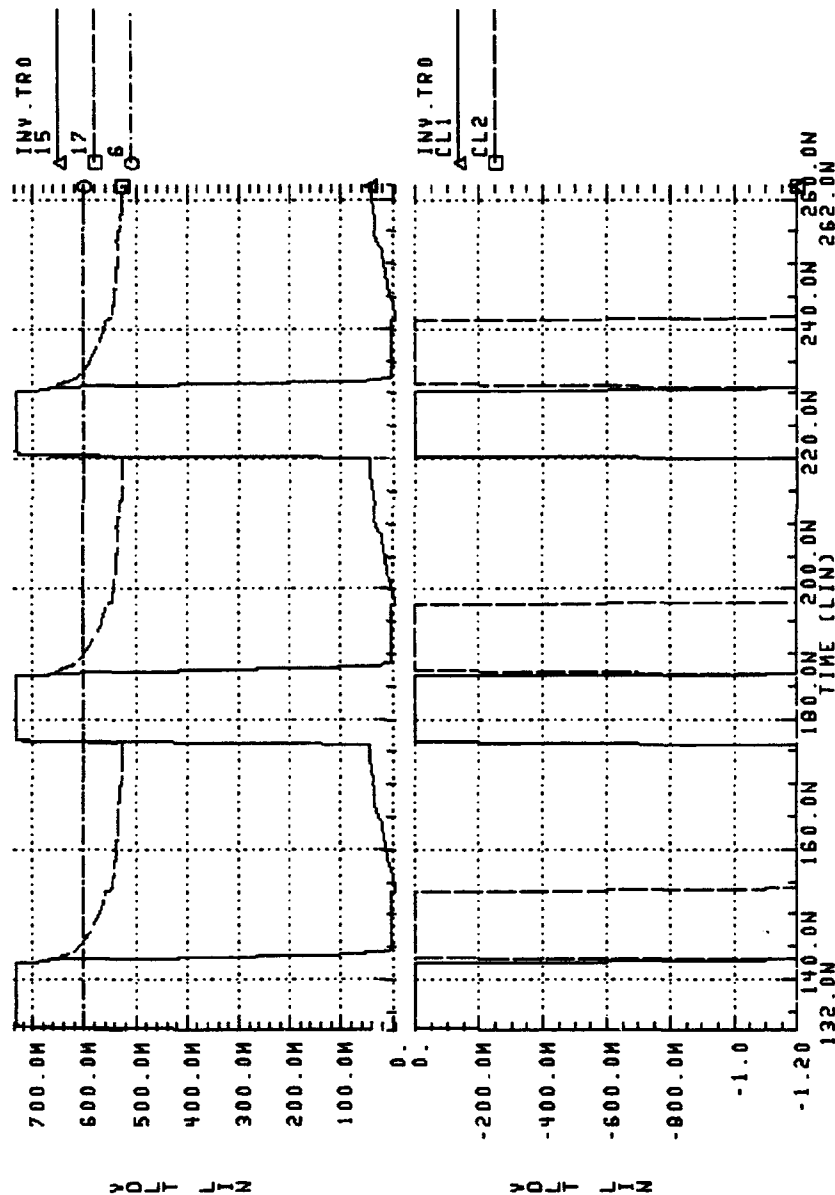




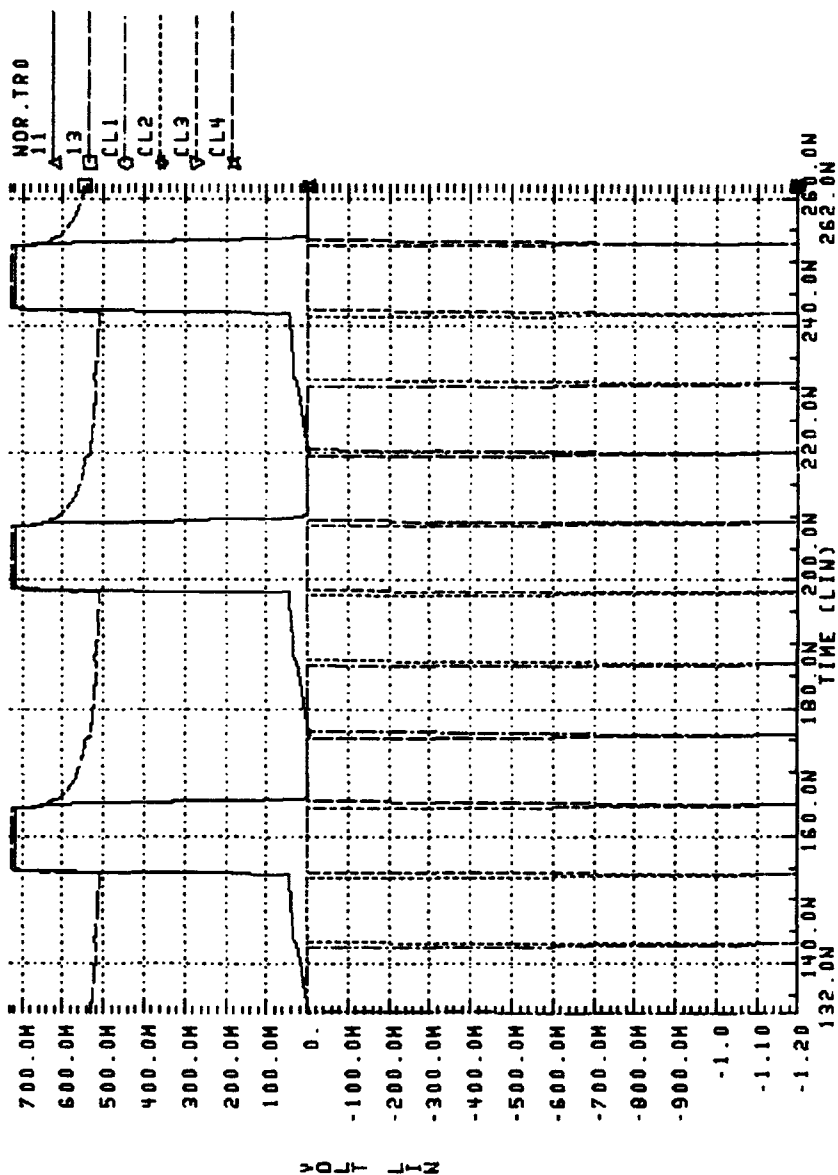
VITESSE HGAAS3 FOML INVERTER  
30-SEP93 15:35:38



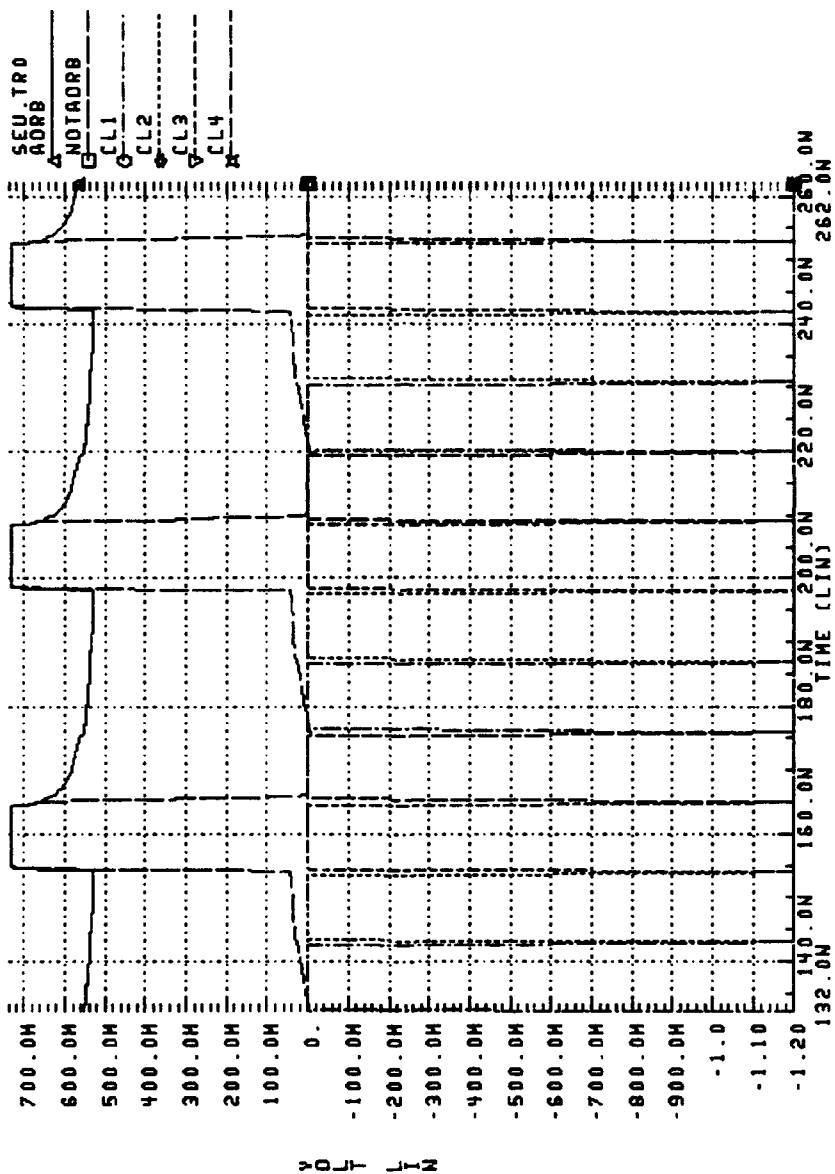
VITESSE HGAS3 FOML INVERTER  
30-SEP93 15:35:38



VITESSE HGAAS3 FDM NOR GATE  
30-SEP93 17:28:32

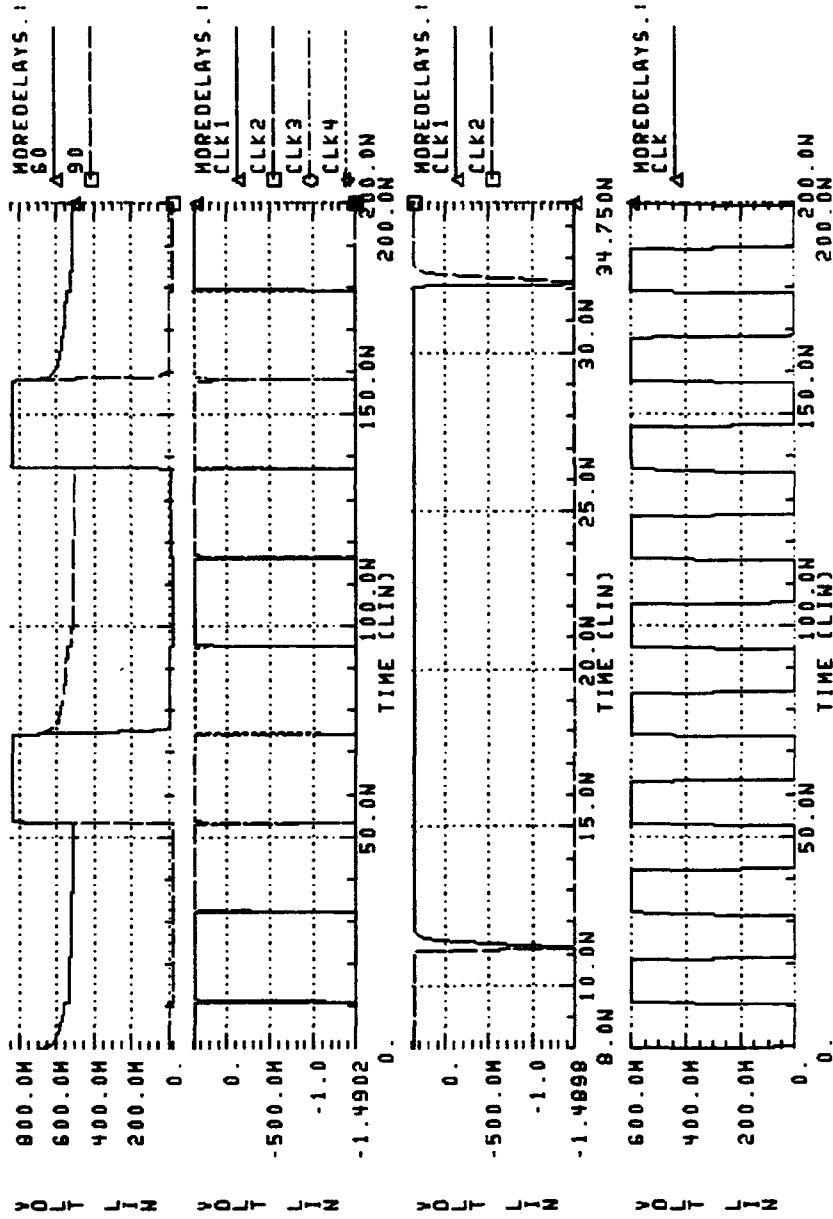


VITESSE HGAAS3 FDWL SEU TEST CIRCUIT  
30-SEP93 18:24:17



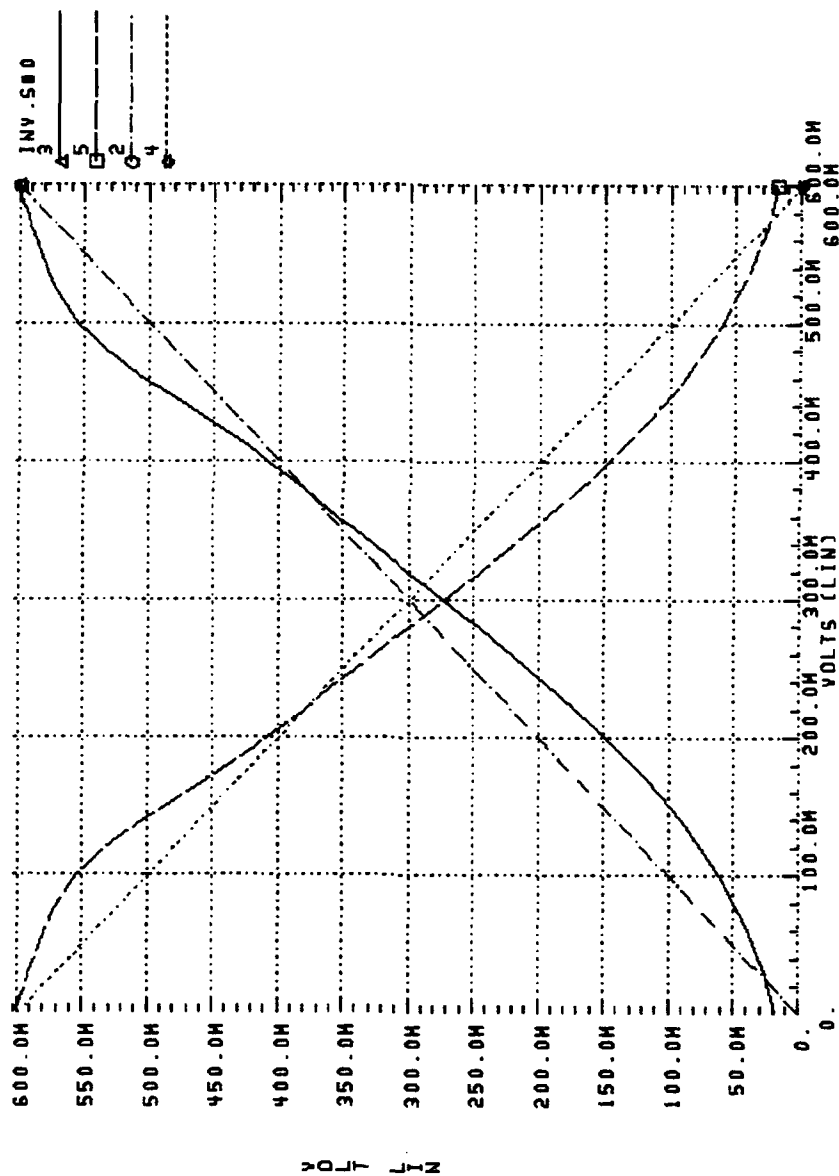
## DCFL FOUR PHASE CLOCK GENERATOR DRIVING FOML FLIP-FLOP

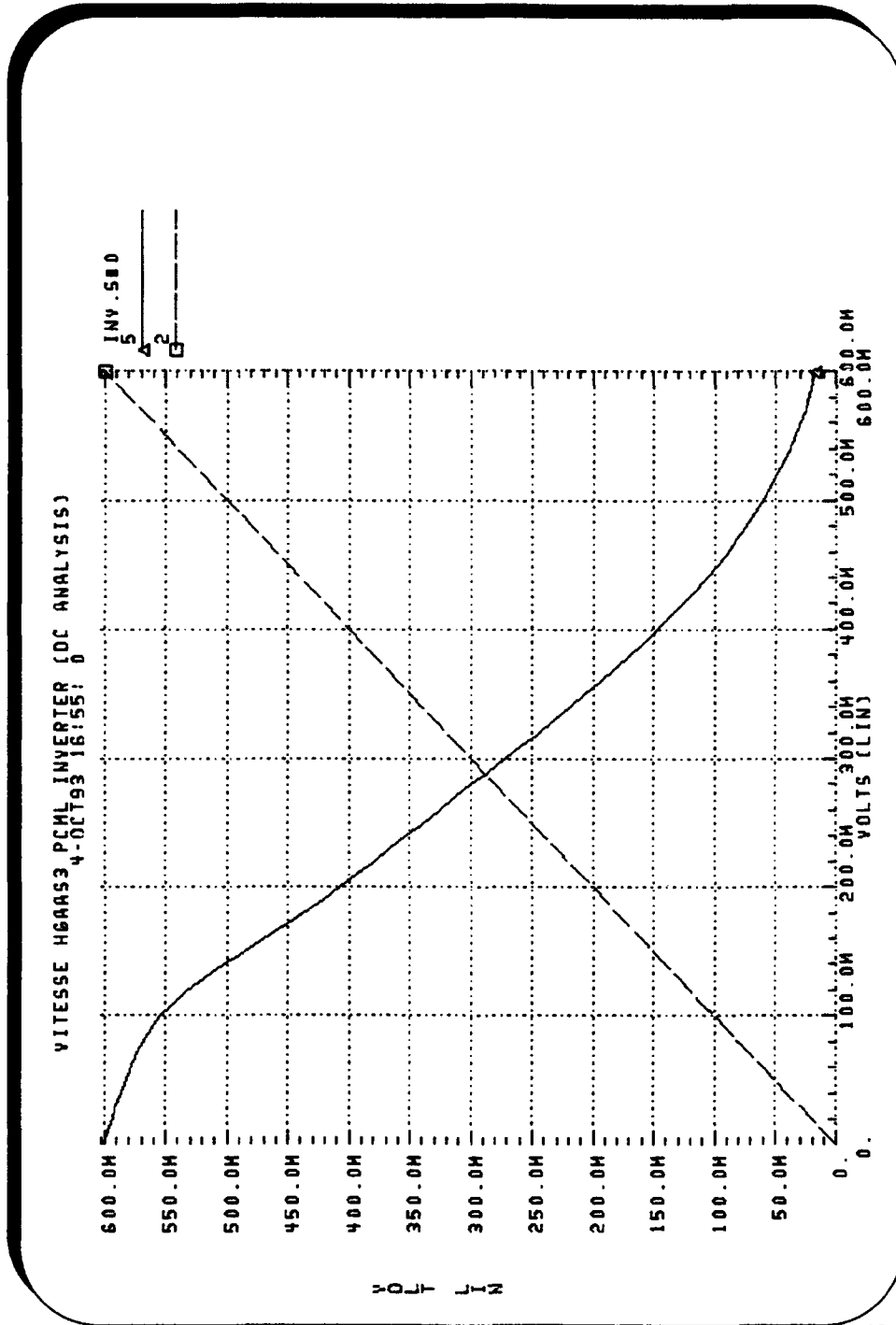
18-OCT93 22:14:14

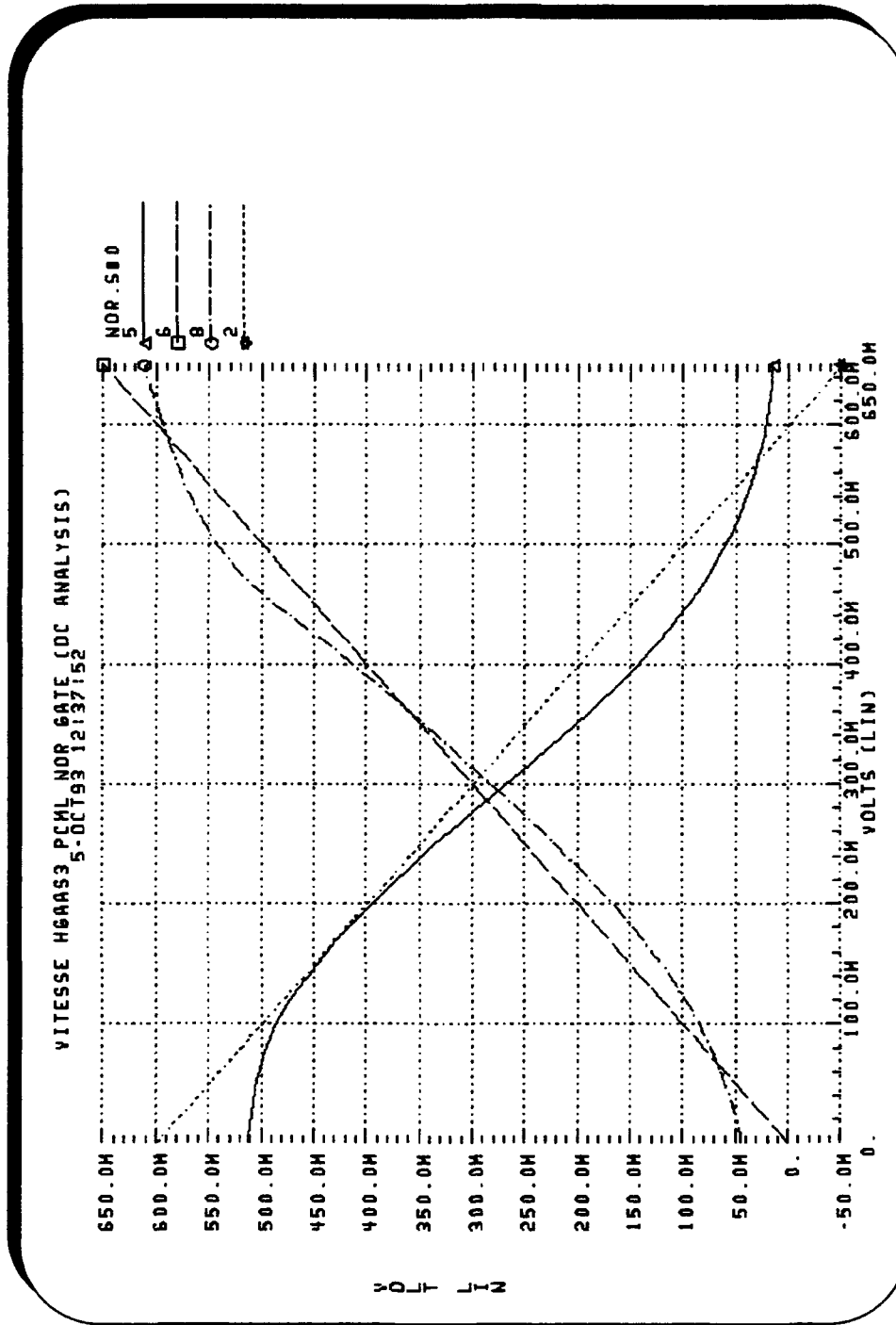


# VITESSE HBAAS3 PCML INVERTER (DC ANALYSIS)

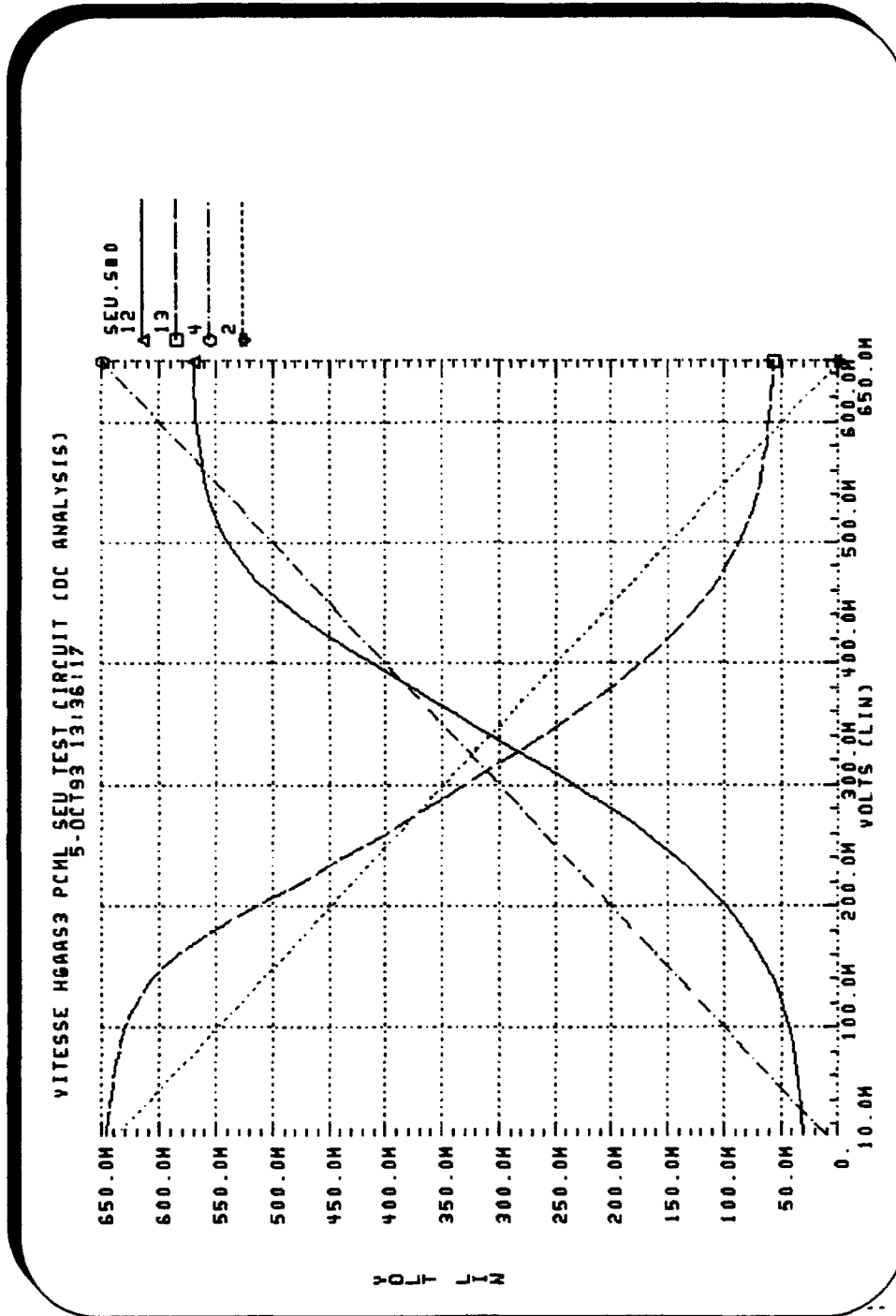
4-00193 16:55: 0



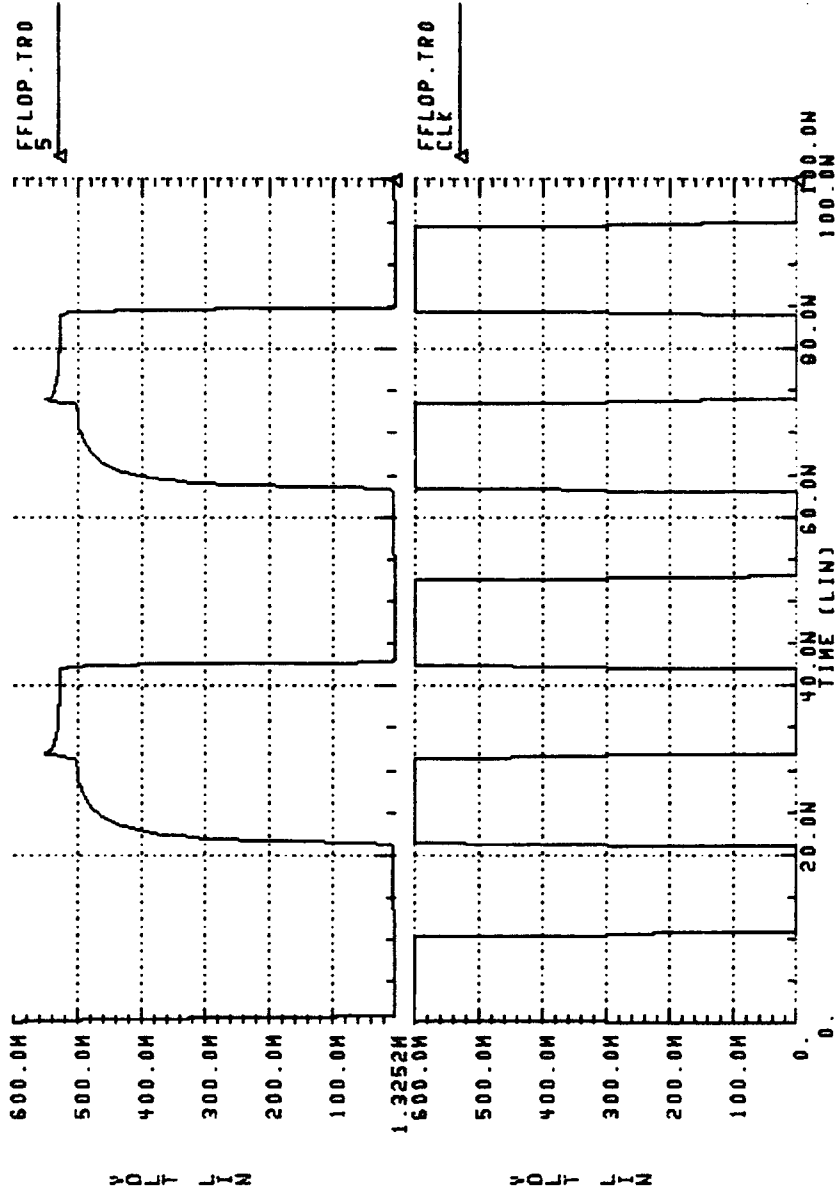




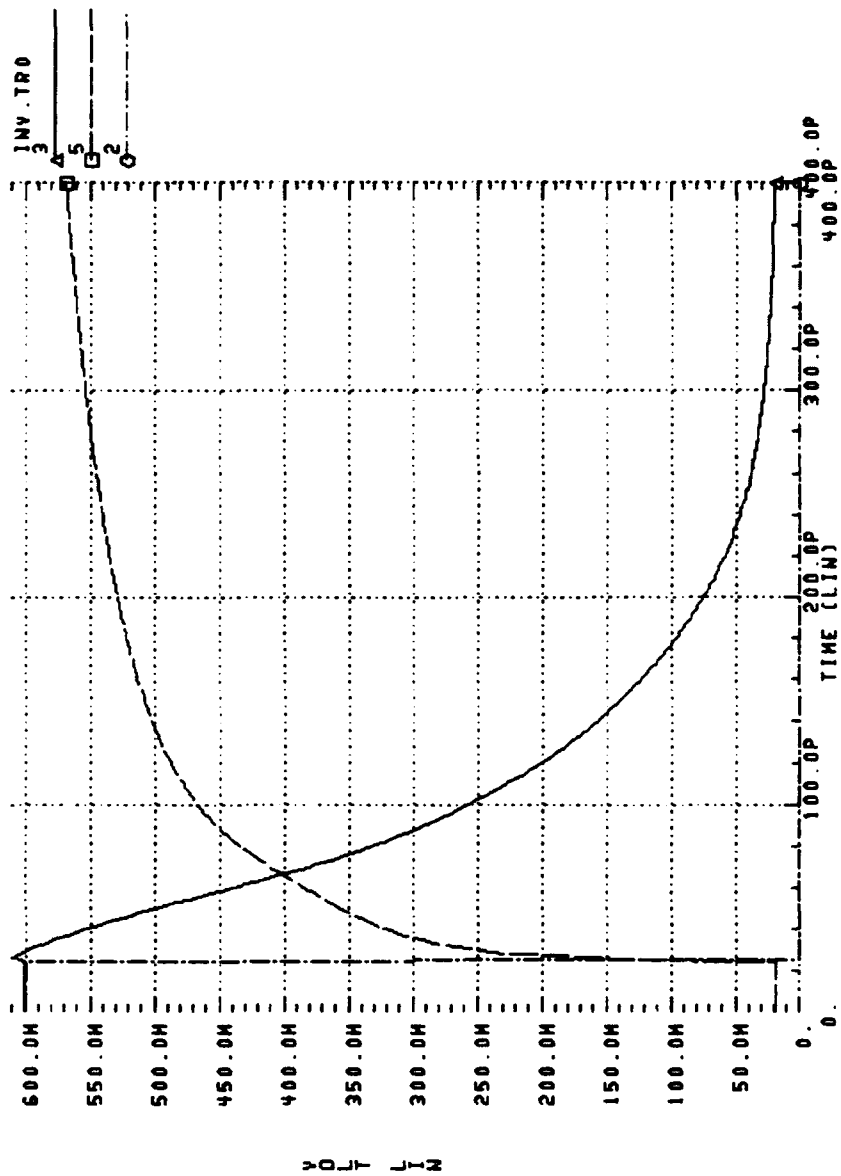




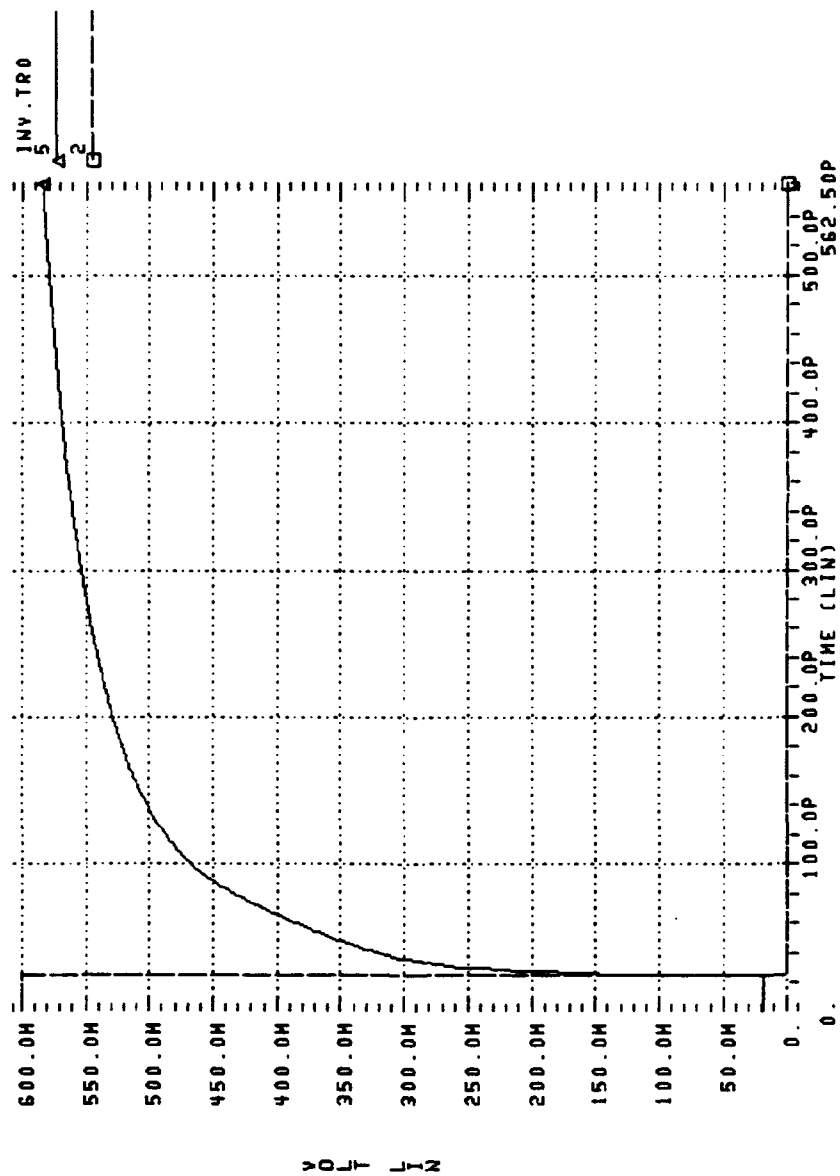
VITESSE HGAAS2 PCWL FLIP-FLOP  
5-01793 151 8125



VITESSE HBAAS3 PCML INVERTER (TRANSIENT ANALYSIS)  
6-OCT93 17:22:43

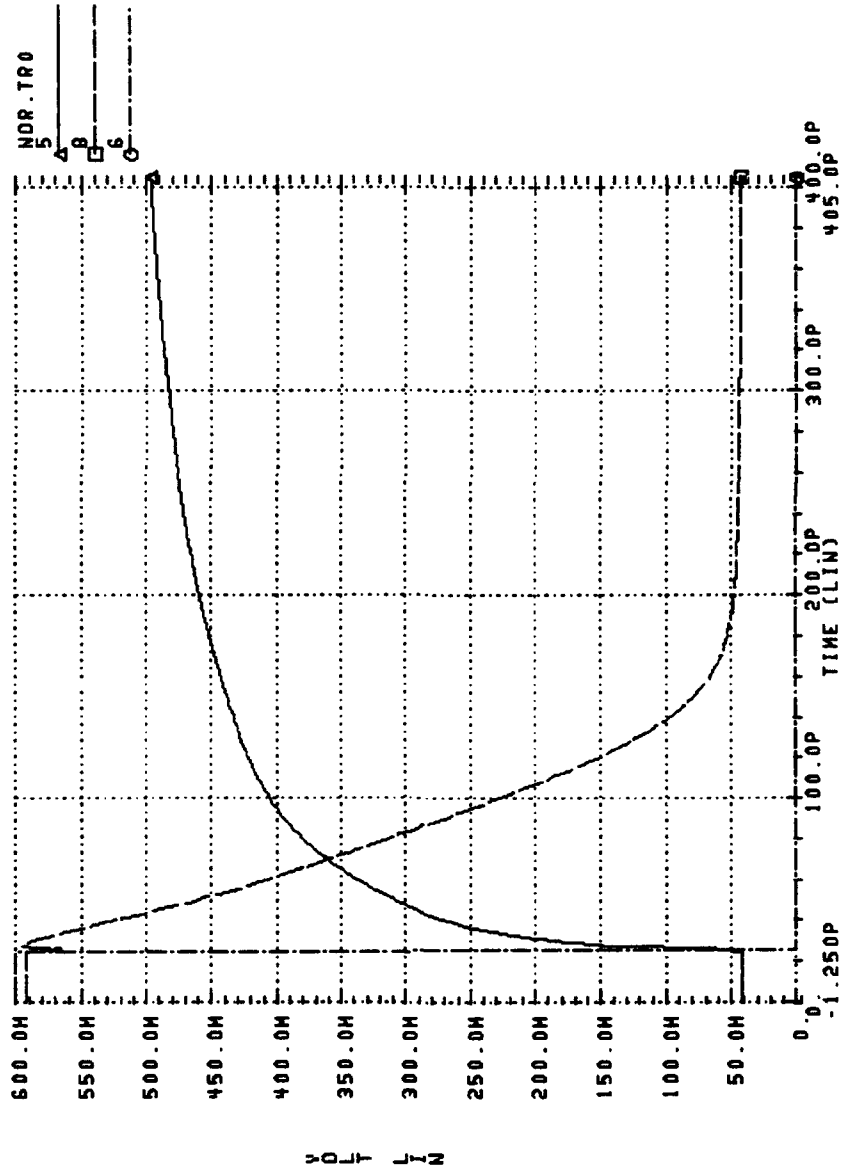


# VITESSE HGAAS3 PCWL INVERTER (TRANSIENT ANALYSIS) 6-00193 17:15:19

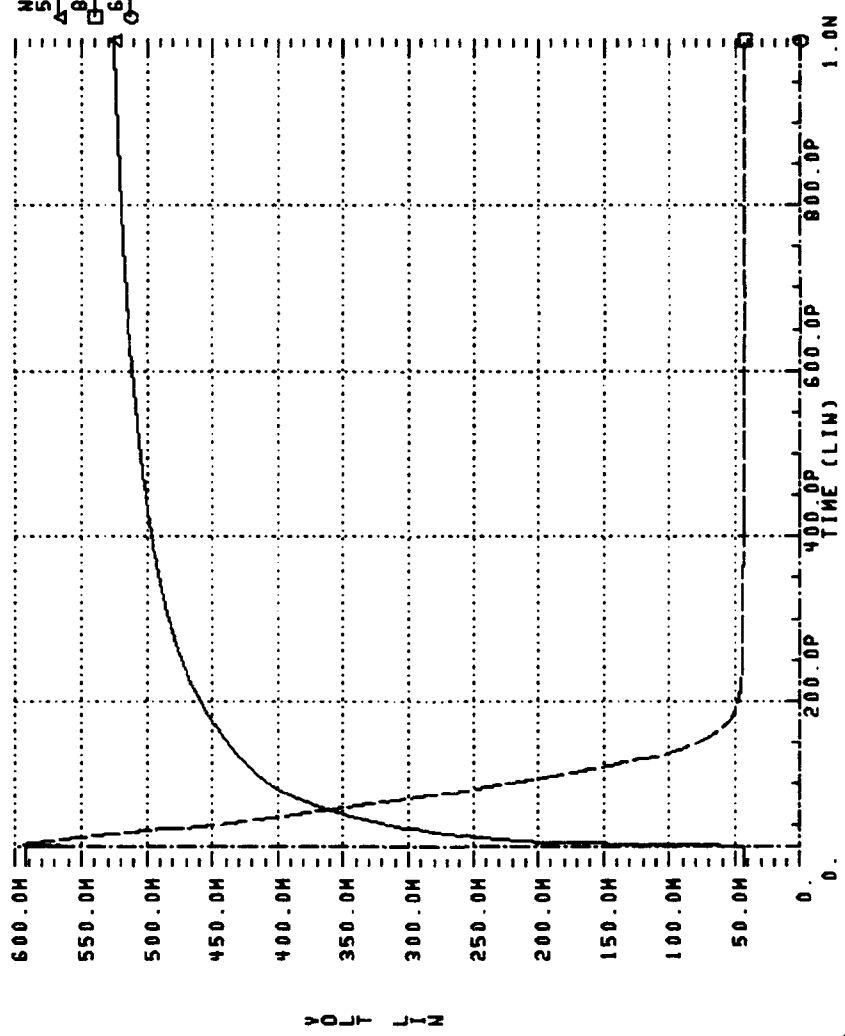


VITESSE H6AAS3 PCML NOR GATE (TRANSIENT ANALYSIS)

8-OCT93 1713:00

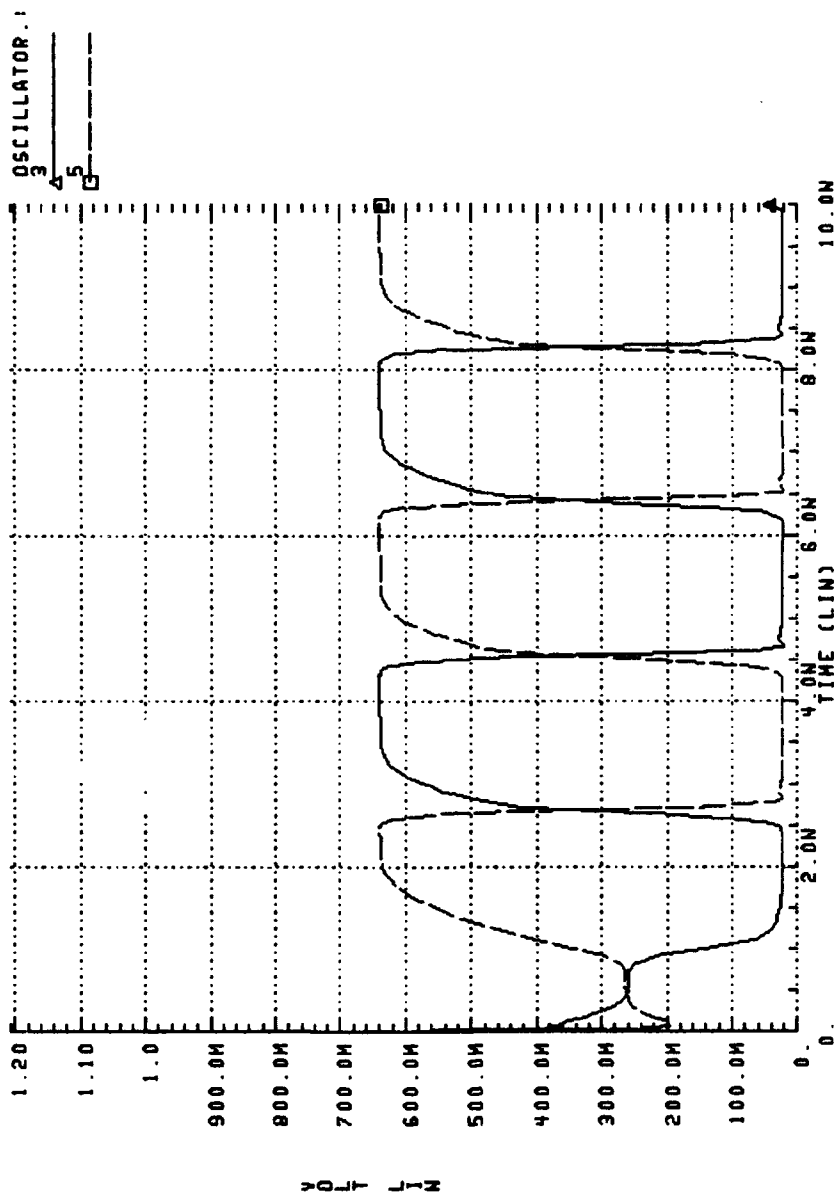


VITESSE HGARS3 PCHL NOR GATE (TRANSIENT ANALYSIS)  
 6-OCT93 17:31:00

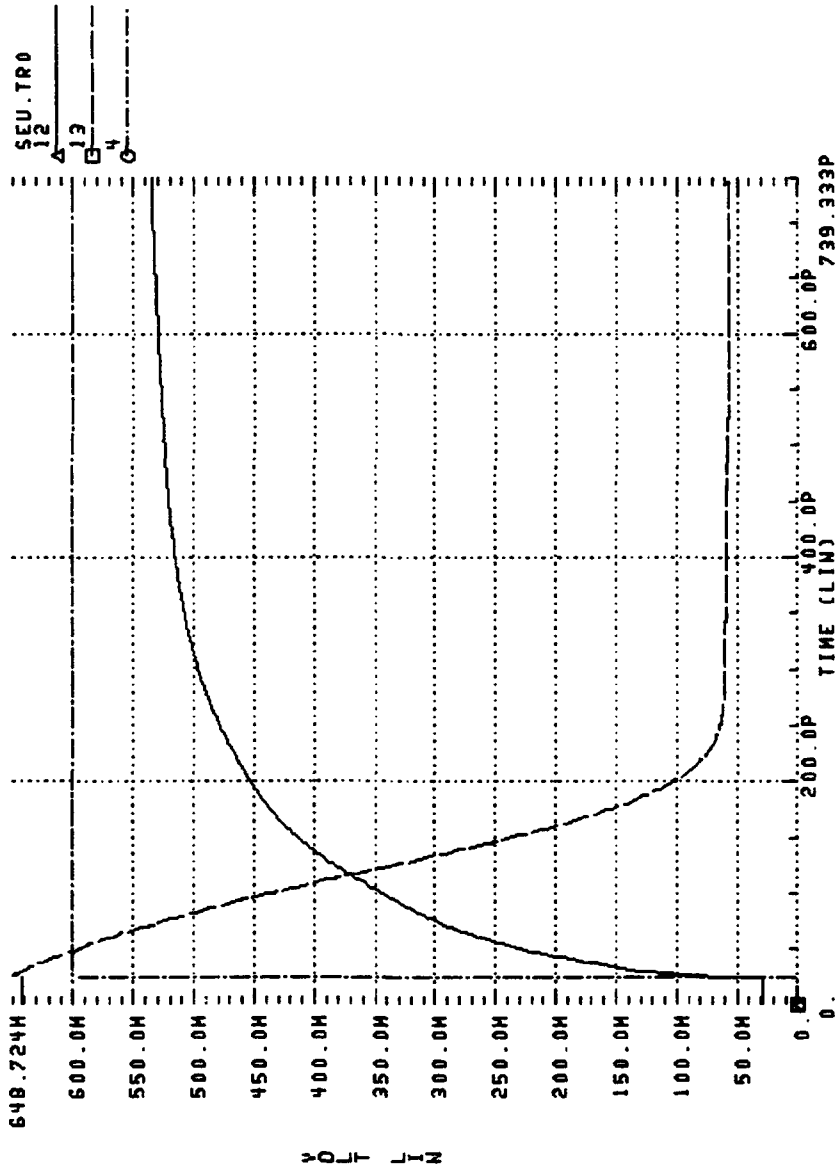


NOR.TRO  
 5  
 4  
 3  
 2  
 1

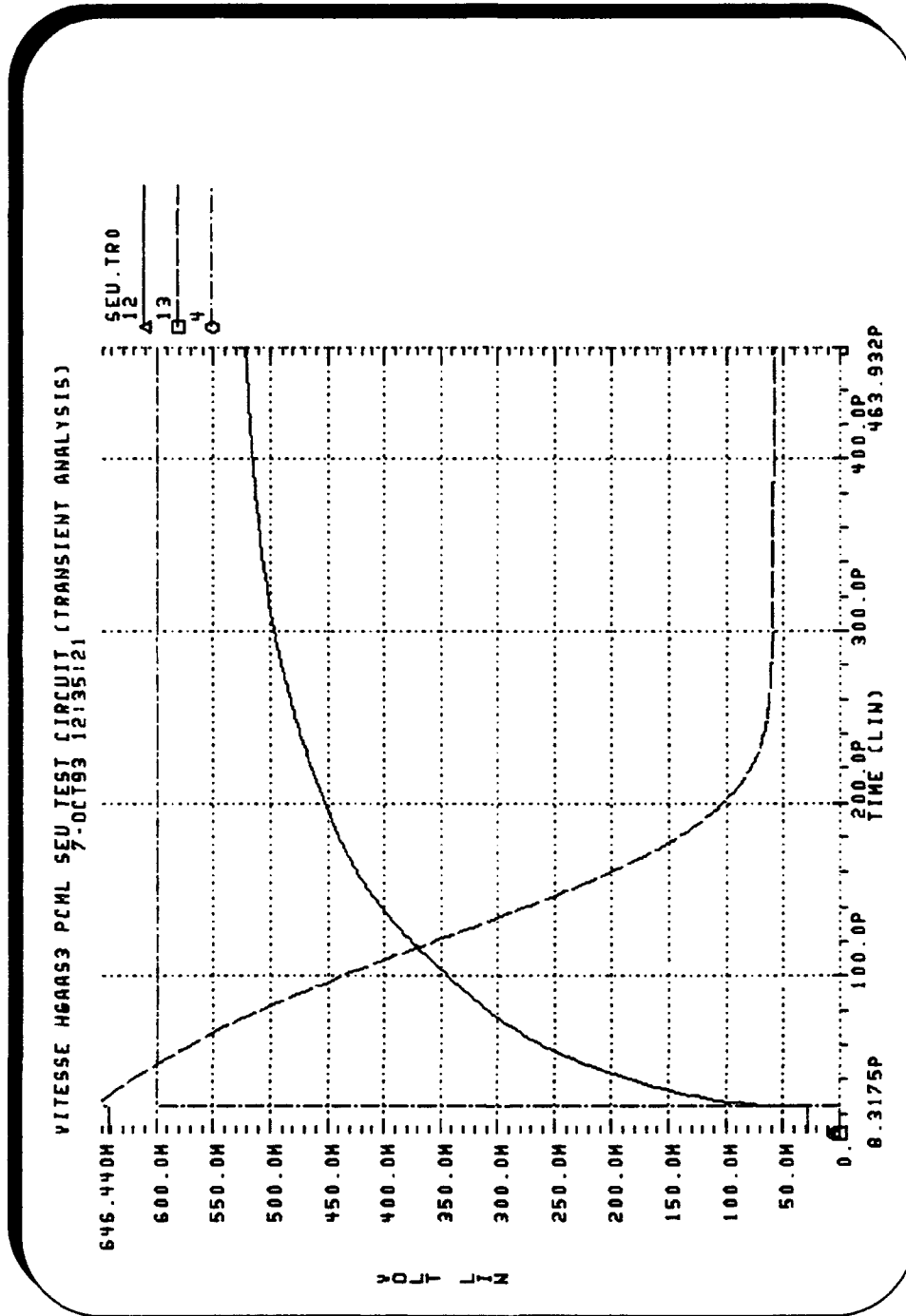
VITESSE H8AAS2 PCH1 RING OSCILLATOR  
29-SEP93 12:44:55

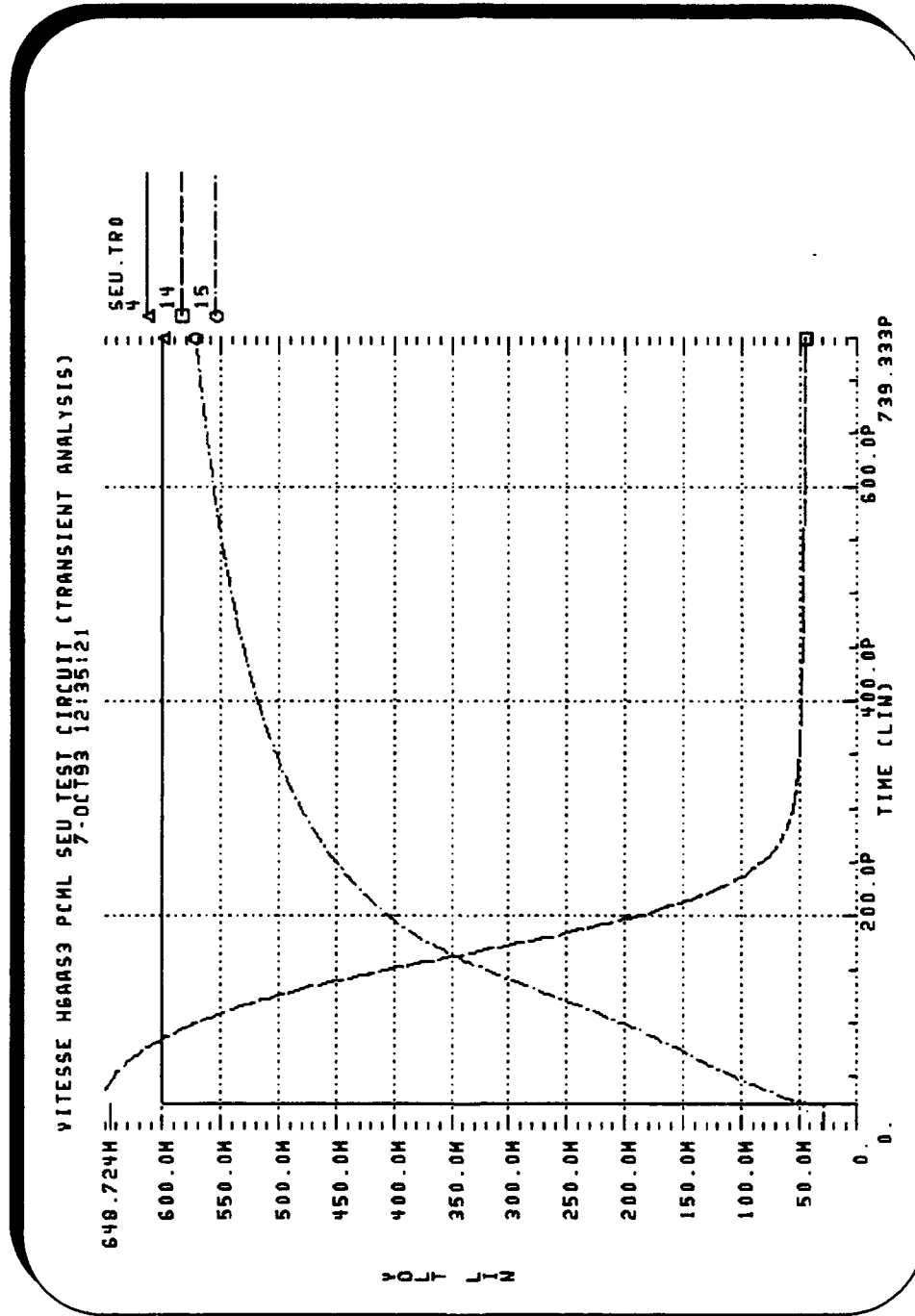


VITESSE H6ARS3 PCML SEU TEST CIRCUIT (TRANSIENT ANALYSIS)  
7-OCT93 12:35:21









## REFERENCES

1. Simons, M., "Radiation Effects in GaAs Integrated Circuits: A Comparison With Silicon," *IEEE GaAs IC Symposium Proceedings*, Pheonix, AZ 1983.
2. Buchner, S. and others, "Charge Collection in GaAs MESFETs and MODFETs," *IEEE Transactions on Nuclear Science*, Vol. 38, No. 6, p. 1370, December 1991.
3. Campbell, A. and others, "Ion Induced Charge Collection in GaAs MESFETs," *IEEE Transactions on Nuclear Science*, Vol. 36, No. 6, p. 2292, December 1989.
4. Nary, K. R. and Long, S. I., "GaAs Two-Phase Dynamic FET Logic: A Low-Power Logic Family for VLSI," *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 10, p. 1364, October 1992.
5. Sedra, A. S. and Smith, K. C., *Microelectronic Circuits*, 3d ed., p. 385-390, Saunders College Publishing, 1991.
6. Meta-Software, Inc., *HSPICE User's Manual*, Version H92, Vol. 1-3, Meta-Software, Inc., 1992.
7. McMorrow, D. and others, "Picosecond Charge-Collection Dynamics in GaAs MESFETs," *IEEE Transactions on Nuclear Science*, Vol. 39, No. 6, December 1992.
8. Fouts, D. J. and others, *Single Event Upsets in Gallium Arsenide Dynamic Logic*, paper to be submitted to *IEEE Transactions on Nuclear Science*, December 1993.
9. Weste, N. and Eshraghian, K., *Principles of CMOS VLSI Design: A Systems Perspective*, pp. 51-54, Addison-Wesley Publishing Company, 1985.
10. University of California at Berkeley, *MAGIC VLSI Circuit Design Software*, Computer Science Division, University of California at Berkeley, CA, December, 1985.

## INITIAL DISTRIBUTION LIST

	Number of Copies
1. Defense Technical Information Center Cameron Station Alexandria, Virginia 22304-6145	2
2. Library, Code 52 Naval Postgraduate School Monterey, California 93943-5101	2
3. Chairman, Code EC Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5121	1
4. Douglas J. Fouts, Code EC/FS Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5121	2
5. Herschel H. Loomis, Code EC/LM Department of Electrical Engineering Naval Postgraduate School Monterey, California 93943-5121	1
6. Lt. Kurt A Wolfe 4750 Valley Drive Helena, Montana 59601	2